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Preliminary Digital Control System Design For the Petite Amateur Navy Satellite (PANSAT)

by

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Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1994

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704

blic reporting burden for this collection of information is estimated to average 1 hour per response, including the time r reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and viewing the collection of information. Send comments regarding this burden estimate or any other aspect of this llection of information, including suggestions for reducing this burden, to Washington headquarters Services, rectorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, d to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.

AGENCY USE ONLY	2. REPORT DATE March, 1994	3. REPORT TYPE AND DATES COVERED Master's Thesis

TITLE AND SUBTITLE PRELIMINARY DIGITAL CONTROL SYSTEM DESIGN FOR THE PETITE AMATEUR NAVY SATELLITE (PANSAT)	5. FUNDING NUMBERS
AUTHOR(S) Leu, David l.	
PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey CA 93943-5000	8. PERFORMING ORGANIZATION REPORT NUMBER
SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSORING/MONITORING AGENCY REPORT NUMBER

. SUPPLEMENTARY NOTES

The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

a. DISTRIBUTION/AVAILABILITY STATEMENT	12b. DISTRIBUTION CODE
Approved for public release; distribution unlimited	A

. ABSTRACT (maximum 200 words)

The Petite Amateur Navy Satellite (PANSAT) project was initiated to demonstrate the feasibility of a quick reaction, low-cost communications satellite incorporating digital communications and a store and forward memory area for the use of amateur radio operators interested in spread spectrum and packet communications. Designed to operate autonomously and under the guidance of a ground station located at the Naval Postgraduate School (NPS) in Monterey, California, it requires a reliable Digital Control System (DCS) to control operations while processing communications and telemetry. This thesis deals with a preliminary hardware design for the DCS and related subsystems. In addition to the design process, individual components were selected which were deemed suitable for the space environment while operating under project constraints of limited power and a desire to create a system using off-the-shelf devices capable of handling temperature and physical constraints equivalent to MIL-STD-883. Reliability, redundancy, and flexibility were requirements of the DCS design.

. SUBJECT TERMS PANSAT, Digital Control System, DCS, Control, Hardware	15. NUMBER OF PAGES 83
	16. PRICE CODE

7. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

N 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

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The Petite Amateur Navy Satellite (PANSAT) project was initiated to demonstrate the feasibility of a quick-reaction, low-cost communications satellite incorporating digital communications and a store and forward memory area for the use of amateur radio operators interested in spread spectrum and packet communications. Designed to operate autonomously and under the guidance of a ground station located at the Naval Postgraduate School (NPS) in Montery, California, it requires a reliable Digital Control System (DCS) to control operations while processing communications and telemetry.

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I. INTRODUCTION

A. PANSAT

The Petite Amateur Navy Satellite (PANSAT) project was initiated to demonstrate the feasibility of a quick-reaction, low-cost communications satellite incorporating digital communications, an orbital mailbox, and low probability-of-intercept/low probability-of-jamming communications [Ref. 1: p. 2]. Scheduled to be launched from the space shuttle in 1996 as a payload of opportunity, PANSAT will use half-duplex, spread spectrum UHF packet communications to support an onboard 4 MByte (1 MByte - 10^6 bytes) store and forward mailbox for the use of amateur radio operators interested in relaying digital traffic. Designed to operate autonomously in a low earth orbit, it will have the capability to be controlled by a ground station located at the Naval Postgraduate School (NPS) in Monterey, California. The Digital Control System (DCS), supporting a microprocessor and associated peripherals, provides critical, central control to satellite operations.

B. DIGITAL CONTROL SYSTEM (DCS) OPERATIONAL REQUIREMENTS

Since PANSAT is expected to operate autonomously for long periods of time, a robust hardware design supporting satellite control is crucial. DCS must be capable of rapid multitasking since it may be expected to handle communications with earth, access

the mass storage area (mailbox), process telemetry data and manipulate onboard systems in real time.

Additionally, DCS must have an interface with other modules containing devices necessary for the accomplishment of required operations such as radios, mass storage, telemetry collection and power.

C. DCS RADIATION EXPOSURE

Operating in a relatively benign environment at an orbit of 250 nm (nautical miles) with an inclination of 28.5°, PANSAT can nonetheless expect to encounter radiation which will, over time, degrade operational performance. CMOS chips are especially vulnerable to radiation. In fact, destructive or hard latchup is common in CMOS ICs that are not treated for radiation tolerance and can result in catastrophic burnout failure [Ref. 2: pp. 416-429].

The major source of radiation expected to affect PANSAT comes from electrons and protons trapped in the geomagnetic field, although corpuscular radiation associated with solar flares is possible [Ref. 3: p. 5-1]. The Van Allen belts will be the chief source of continuing radiation for PANSAT and most of the orbit should be below the effects of the belts. At one point off South America, however, in an area of the south Atlantic known as the South American Anomaly, due to a weakening of the earth's magnetic field, the Van Allen belts reach to lower altitudes. Excluding a possible solar flare, this area will dominate the total dose of radiation received by PANSAT, which could be as much as 1000 rad(Si)/year [Ref. 4: pp.2.2-1 to 2.2-4].

While this is a relatively low dose, the failure of only one component on each DCS could conceivably terminate PANSAT usefulness. For this reason, radiation tolerance of critical components weighed heavily in the selection process. Should this prove to be less of a concern in the future, chips were selected which are capable of pin for pin swapout with less tolerant devices.

D. DCS DESIGN REQUIREMENTS

An overriding consideration in the design process was to eliminate the single point of failure of critical systems by providing redundancy where possible. The Space Systems Department at NPS addressed this issue by specifying that a modular approach to design be undertaken and that three critical modules (DCS, mass storage, and telemetry acquisition) be duplicated. The resulting block diagram is shown in Figure 1. This paired modular approach can be accomplished with virtually identical designs for each module, individual modules differing only in two of the connections used to decode the addresses. The modular approach also allows each DCS to access two of the mass storage or telemetry processing modules, increasing overall operational flexibility.

Since only one microprocessor can control the satellite at a time, a mechanism was devised to alternate between DCS modules. Selection of the active DCS is based on a watchdog timer located in the electrical power module. Each DCS microprocessor has a programmable timer output that pulses the watchdog timer periodically when the DCS is active. If the active DCS microprocessor timer fails to pulse the watchdog on schedule, the electrical power module will remove power from the current DCS and

switch to the alternate. Since the timer is programmable, NPS ground control can also trigger the DCS switch when desired.

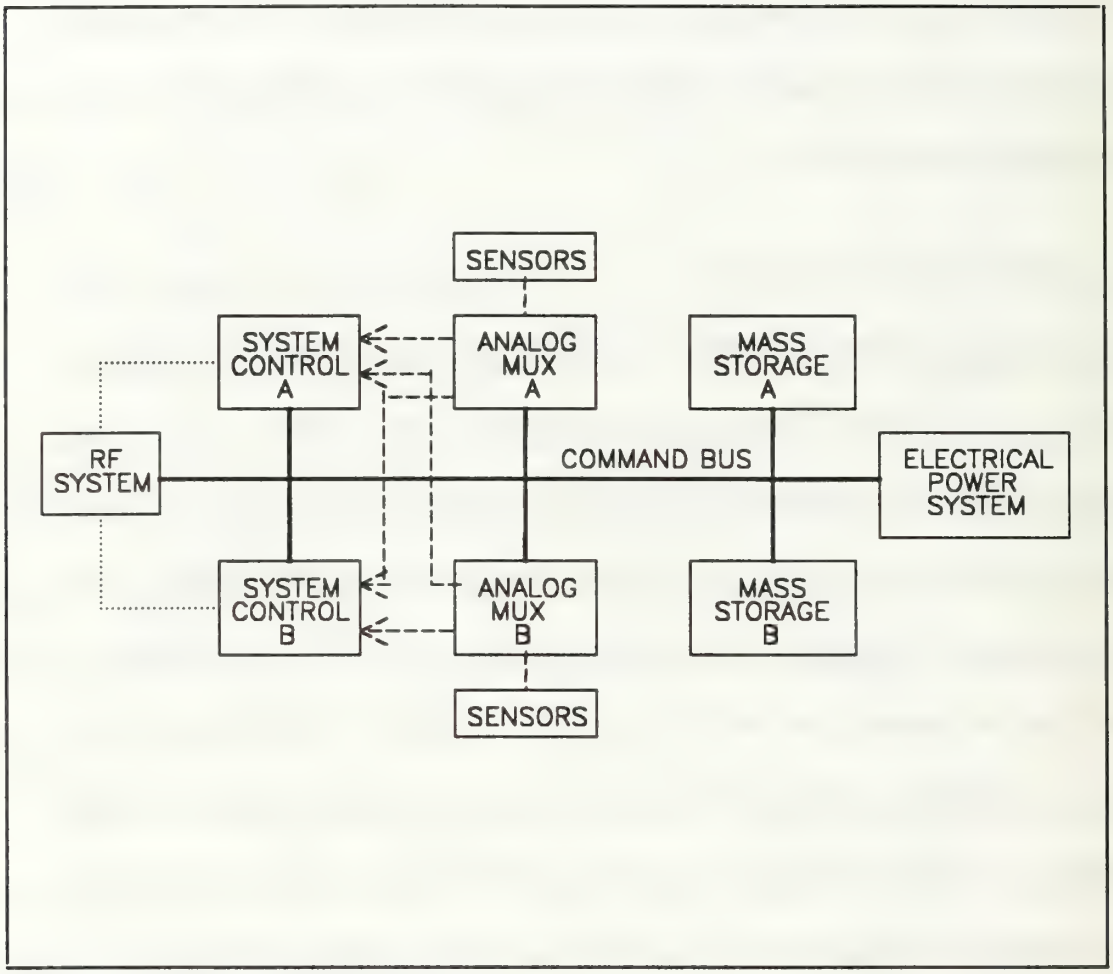

Figure 1 PANSAT Block Diagram

The modular design approach necessitates a command bus architecture between modules. Specified as a 25-line connector, this bus carries virtually all contact between the modules from power to data. It is only bypassed by external connections between each DCS and the RF system and each DCS and input lines from the telemetry processing modules (Analog Mux A and B). The bus approach, as implemented, allows only 8 bits of data at a time to be sent to a specified module and consequently is

relatively slow compared to 16-bit operations on the DCS module. However, it eases considerably wiring connectivity between separate boards aboard PANSAT.

System reliability is another important consideration, mitigated by a desire to keep costs down for what is essentially a short-term satellite. Space-certified parts were deemed to be difficult to obtain and excessive in cost, thus individual critical components were selected which were capable of being acquired in MIL-STD-883 grade and radiation tolerant/hardened parts selected where the device location in DCS operations was considered especially sensitive (Section I.C germane).

A prime limitation in component selection is the fact that PANSAT is operating under tight power constraints and there is almost a direct correlation between component hardening and power requirements. A balance had to be struck in part selection, although since loss of the DCS modules would effectively terminate satellite operation, hardened components appear throughout the design.

A single-chip approach to the communications issue of spread spectrum demodulation was specified and this drives the supporting functional design.

An initial design for the DCS was constructed by Ashe [Ref 5], and the interrelationship between the functional sections of that design is demonstrated in Figure 2. While apparently feasible, and containing several unique features, this design was proposed prior to current PANSAT requirements and is no longer applicable. The current DCS block diagram is shown in Figure 3.

E. SCOPE OF THESIS

This thesis deals primarily with the hardware necessary to create a functioning DCS and deals with software only insofar as necessary to support peripheral device access.

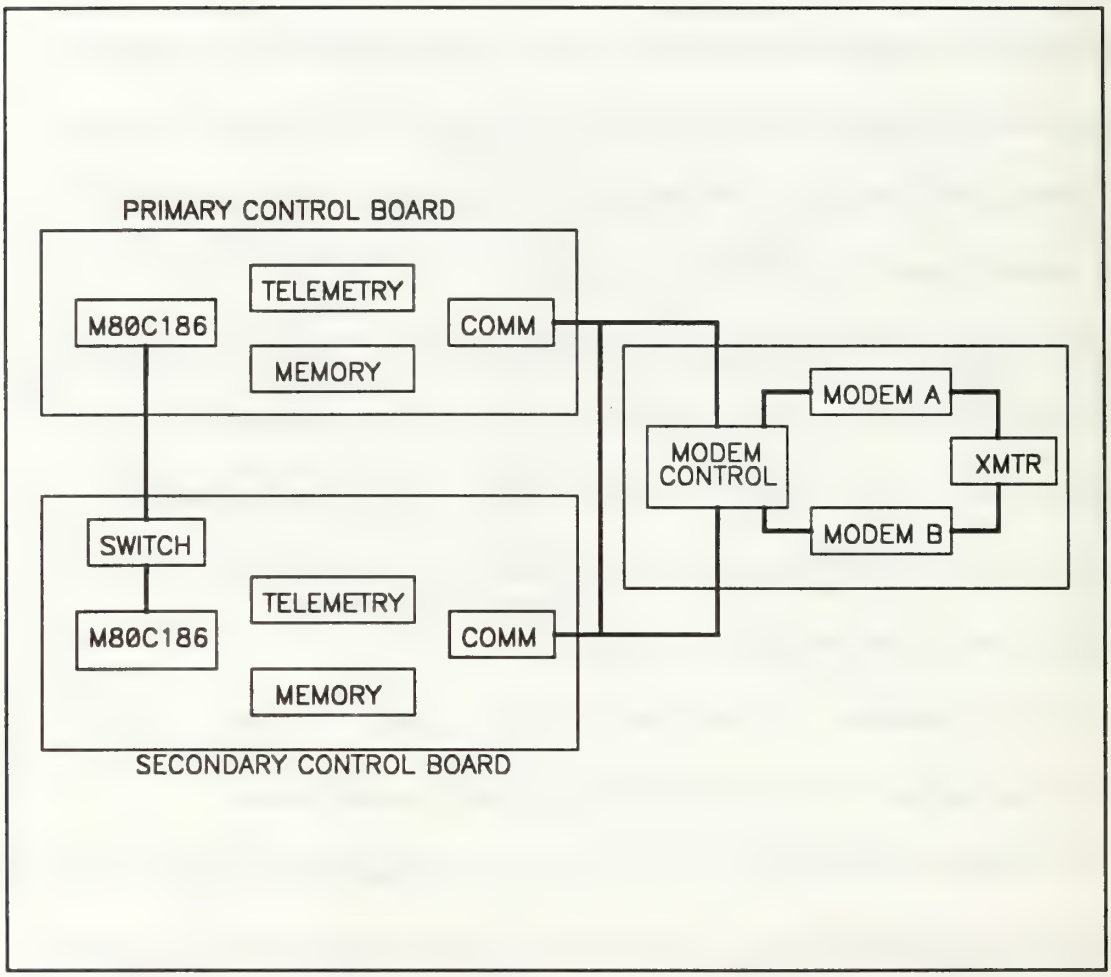

Figure 2 Preliminary DCS Design [Ref. 5: p. 2]

While hardware and specific design requirements are still evolving, an attempt has been made to generate a design for the DCS that supports current requirements and is flexible enough to be transparent to most changes. Where possible, components were

selected with excess capability for potential changes, if this could be done with minimal impact to power requirements and board space limitations. Additionally, selected components adhere to industry standards and are available at reduced or increased levels of radiation tolerance from various manufacturers on a pin for pin compatible basis.

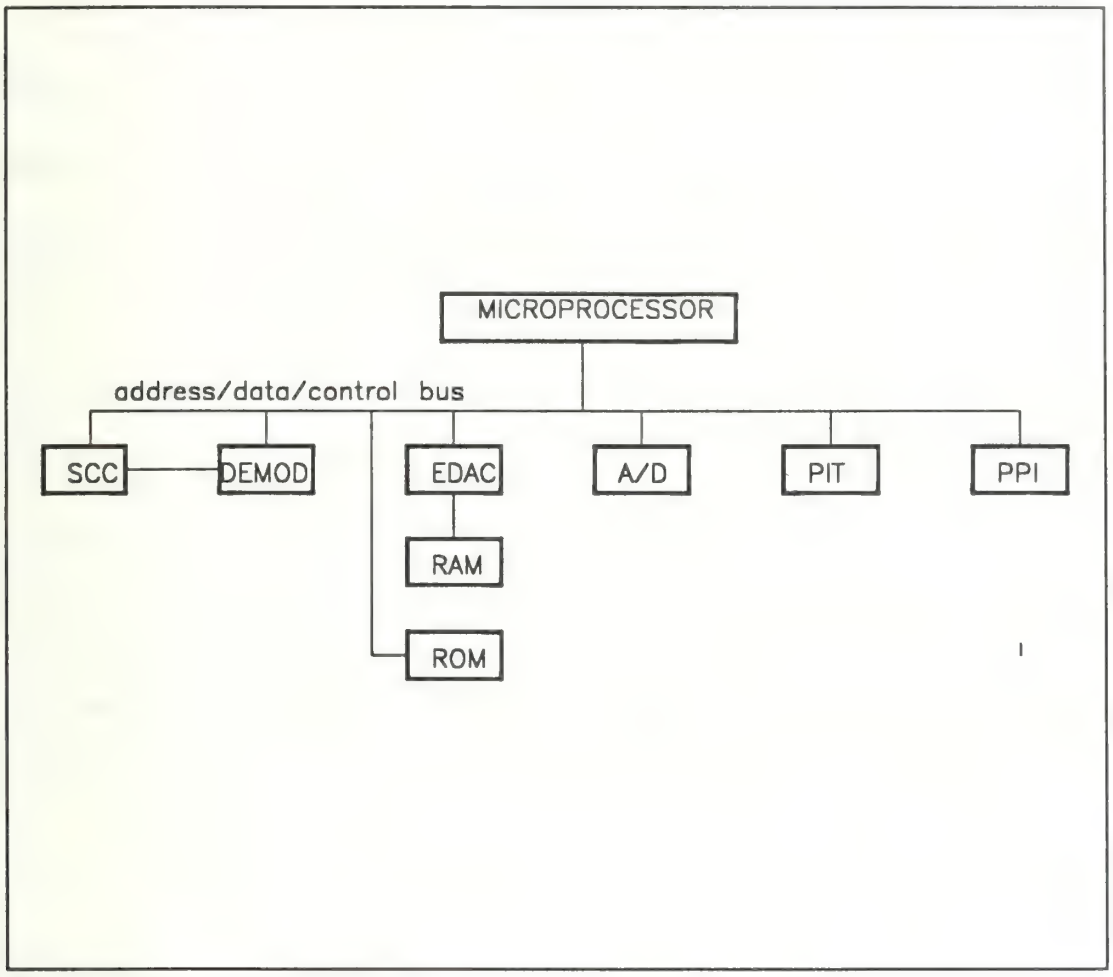

Figure 3 Current DCS Design

Section II is a description of the implementation of a command bus interface, allowing the DCS to access the individual modules and pass control, addressing and data where required. Microprocessor selection and basic operation is also discussed in this

section. Central to the command bus interface design is selection and operation of a programmable peripheral interface (PPI).

Section III is a description of the system memory operation. The microprocessor can directly address 1 MByte of memory and a mechanism was devised for overlapping a variable amount of ROM (read only memory) onto 1 MByte of RAM (random access memory), allowing final determination of ROM requirements to be made at some future date with minimal impact to hardware design. Because of the critical nature of system RAM, an error detection and correction (EDAC) circuit was implemented allowing for single bit correction and double bit detection of errors during a read operation.

Section IV addresses an analog to digital converter (ADC) capable of interfacing with the analog multiplexer modules, which are central to onboard collection of telemetry data.

Section V functionally addresses a basic design for processing the spread spectrum communications. Because of a lack of technical information on a specified component of this design, the spread spectrum demodulator, only a preliminary approach to the design was conducted.

II. COMMAND BUS CONTROL ARCHITECTURE

A. GENERAL

The DCS microprocessor must have the capability of controlling a number of peripheral devices, more so than the number of peripheral control lines available on microprocessors suited for this design. To get around this limitation, a programmable peripheral interface (PPI) was selected with sufficient capability to handle current requirements and surplus capability to respond to currently unforeseen requirements, if necessary. This microprocessor/PPI construct, augmented by latches and transceivers, serves as the control architecture for the command bus. Selection criteria and operational use of these command bus control components follow.

B. COMMAND BUS CONTROL DESIGN

1. Intel M80C186 CHMOS High Integration 16-bit Microprocessor

a. General Selection

The microprocessor serves as the principle component of the DCS and as such, its selection is critical. While a number of new technology devices of sophisticated operation are available, their enhanced capabilities would be essentially unused since the basic control functions of PANSAT can be satisfied by a more basic device. The M80C186 [Ref. 6: pp. 9-1 to 9-59] is shown in Figure 4. Additionally,

enhanced capability usually is tied to a concomitant increase in power consumption, a significant factor in device selection. Principle selection criteria included:

1. Available in MIL-STD-883 grade
2. Radiation tolerant
3. Low power design with power save logic
4. Ability to satisfy PANSAT multitasking requirements
5. Proven dependable performance

b. Specific Features

Other criteria also factored into the selection of the M80C186, enhancing its ability to perform PANSAT DCS functions. Operating at 10 MHz, the microprocessor is fast enough to handle real time satellite requirements as currently specified. Should this prove to be inadequate, the M80C186 is also available in a 12.5 MHz version, and other variants are available in speeds up to 20 MHz, albeit at higher power consumption rates.

The M80C186 also has the ability to directly address 1 Mbyte of memory, a capability which is used for system memory (ROM and RAM). Since the microprocessor is a 16-bit device, some manipulation is required to generate the 20-bit address necessary for direct addressing. This is accomplished by truncating a 16-bit base segment to 4 bits and concatenating a 16-bit offset value to yield an address for the 20 address lines, AD0-AD15 and A16-A19 (see Figure 4). Addressing of the additional 4 Mbyte of memory used for mass storage functions is achieved by the use of a PPI on the mass storage module.

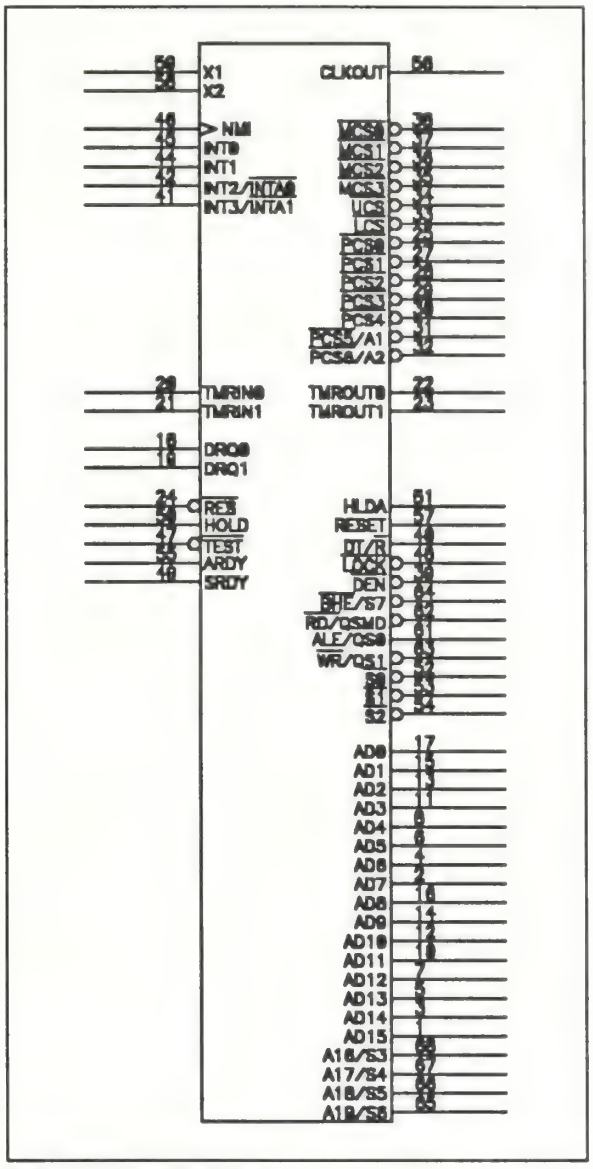

Figure 4 M80C186

Peripheral chip select (PCS) logic allows the direct control of up to seven peripherals, or direct control of 5 peripherals and 2 software programmable latched signals. The second option was implemented for PANSAT. Table 2.1 contains PANSAT microprocessor PCS assignments.

TABLE 2.1 PERIPHERAL CHIP SELECT (PCS) ASSIGNMENTS

PCS	USAGE
PCS0	Serial comms controller
PCS1	A/D converter
PCS2	Programmable Peripheral Interface
PCS3	Programmable Interval Timer
PCS4	Spread Spectrum Control
PCS5	latched A1
PCS6	latched A2

A programmable wait-state generator is available as part of the integrated chip select logic for both memory and peripherals. This eliminates the requirement for external delay circuitry in addressing memory, which is contingent upon memory speed and error detection and correction circuitry for system memory, and memory speed and address transfer delays in mass storage, and peripherals, which is contingent upon functional requirements.

Capable of servicing interrupts, which can be generated by hardware or software, the M80C186 interrupt controller can merge these requests to be serviced as required and on a priority basis. A non-maskable interrupt can be used to activate a power failure routine or respond to an indicated flag from error detection and correction (EDAC) circuitry. By tracking the number and type of EDAC flags generated from system memory use, it may be possible to plot and calculate areas of high radiation and decreased system reliability as a function of orbit location, or track the overall decrease in system reliability as the satellite ages.

Two independent direct memory access (DMA) channels significantly aid in maintaining system speed while data is being transmitted or received by the RF system or the ADC. System specifications for communications have a data transfer rate set at 1200 baud, a speed which would significantly hamper DCS operations if dedicated microprocessor control was required. However, with the use of a serial communications controller utilizing interrupt/polling operations, and with the M80C186 and DMA channels allowing transfer of data between memory and I/O, the impact of communications data transfer at this rate is minimized.

Three integral and programmable 16-bit timers are used in the selection of which DCS is to be active and can be used in the collection of telemetry data. One timer is dedicated to determining which DCS is active. This is accomplished by the periodic triggering of a watchdog timer aboard the electrical power system by the active DCS. Should the DCS microprocessor fail, or upon direction from the ground halting the timer, after a specified time the watchdog timer would transfer power, and thereby control, to the other DCS.

2. Intel 82C55A Programmable Peripheral Interface (PPI)

a. General Selection

The M80C186 has insufficient capability to address more than seven peripherals directly. The standard design technique around this microprocessor limitation is the incorporation of a PPI into circuit design. The PPI selected for PANSAT is the

Intel 82C55A PPI [Ref. 7: pp 3-100 to 3-146] as shown in Figure 5. Principle selection criteria for this device include:

1. Available in extended temperature range
2. Radiation tolerant
3. Low power design
4. Designed for use with Intel microprocessors

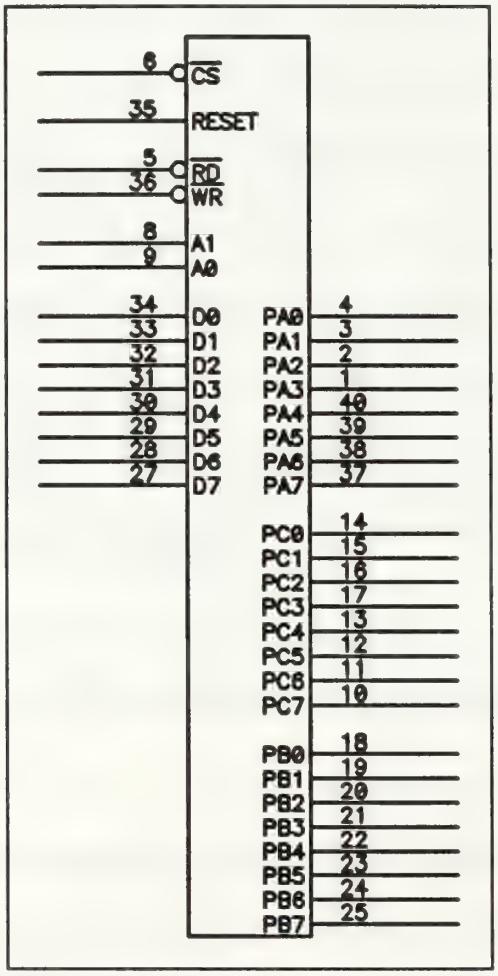

Figure 5 82C55A

This chip is available in an extended industry temperature range but is not available in a MIL-STD variant. Should this device prove unsuitable, a possible alternative is the Harris HS-82C55ARH [Ref. 8: pp. 9-74 to 9-93]. The Harris chip adheres to the same 8255A industry standard as the Intel device and is available radiation hardened and in the military temperature range. It is somewhat slower than the Intel chip, zero wait states at 8 MHz for the Intel versus at 5 Mhz for the Harris, and requires slightly higher power. However, with respect to pinout and programming, a one-for-one substitution is possible.

b. Operation

PANSAT design mandates control of a number of external modules and individual devices, more so than the seven integral peripheral control lines of the microprocessor. The fully programmable 82C55A has the ability to handle all current peripheral control requirements with excess capability to accommodate any future requirements that may develop. Future requirements could easily be accomplished by minor software modifications aboard the DCS and the addition of control lines from the device to the command bus.

No external logic is required to interface peripheral devices since system software programs the functional configuration of the PPI by means of a series of write commands to PPI control registers. The selection of one of the three ports or the control word registers of the PPI is accomplished by the input signals shown in Table 2.2 .

TABLE 2.2 PPI ADDRESSING [REF 4: p. 3-125]

A1	A0	RD	WR	CS	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
					Disable Function
1	1	1	0	0	Data Bus - Control
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

Three modes are available for 82C55A operation:

1. Mode 0 - Basis I/O
2. Mode 1 - Strobed I/O
3. Mode 2 - Bi-directional bus

A combination of Mode 2 and Mode 0 (output) was selected as most suitable for PANSAT command bus control operations. In this mode combination, port A is used as a bi-directional bus with 5 pins of port C acting as a control and status port for port A, and port B used as an output port. The other three pins of port C (PC0-PC2) can be defined as either input or output as required, although current planning indicates a probable configuration as output (e.g., one bit each used for EDAC enable/disable

during system boot, gate enable for programmable interval timer used for the radio transmitter, and mux A/B selection for the A/D). Assuming pins PC0-PC2 are to be used as output, this necessitates the use of control word 11XXX000 for the PPI, where X's are don't care values (see Figure 6).

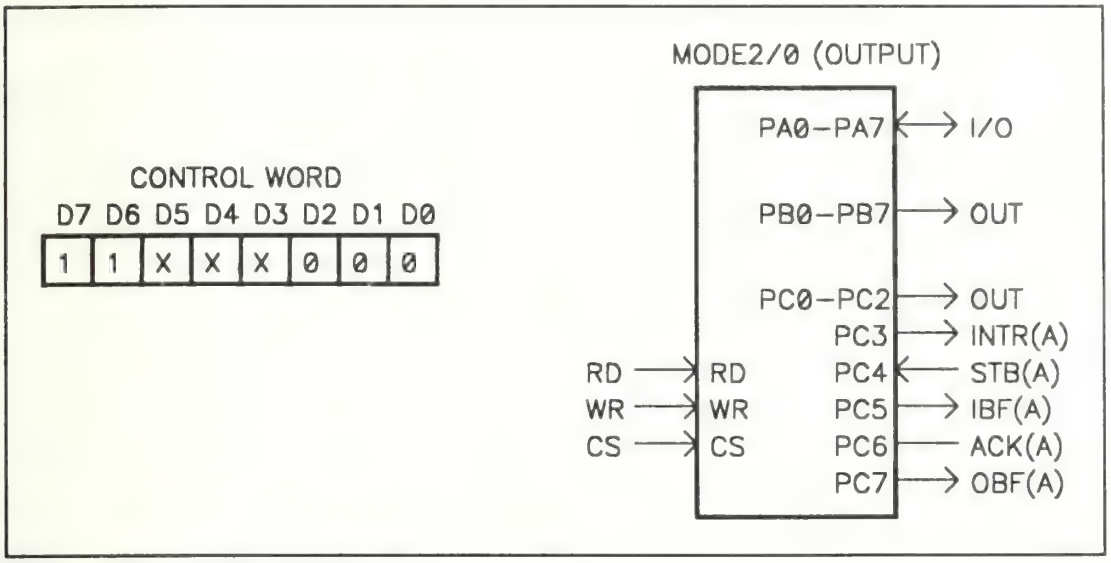

Figure 6 PPI OPERATION

While port A is used to pass address or send/receive data information to/from the appropriate peripherals, port B is used to pass the actual peripheral selection and operation information (Table 2.3), and port C is used for PPI/microprocessor control information (Table 2.4).

It can be seen in Table 2.3 that addresses of paired modules (e.g., DCS A and DCS B) differ only in the most significant digit, making decoding of the address at the module a matter of interchanging two wires on the address decoder.

TABLE 2.3 PPI PERIPHERAL ADDRESSES

PB3	PB2	PB1	PB0	MODULE
0	0	0	0	RF
0	0	1	0	DCS A
1	0	1	0	DCS B
0	1	0	0	ANALOG MUX A
1	1	0	0	ANALOG MUX B
0	1	1	0	MASS STORAGE A
1	1	1	0	MASS STORAGE B
1	0	0	0	ELECTRICAL POWER

TABLE 2.4 PPI PORT C OPERATIONS

PORT C	OPERATION
PC0	I/O
PC1	I/O
PC2	I/O
PC3	INTERRUPT REQUEST (PORT A)
PC4	STROBE INPUT (PORT A)
PC5	INPUT BUFFER FULL (PORT A)
PC6	ACKNOWLEDGE /RELEASE DATA (PORT A)
PC7	OUTPUT BUFFER FULL (PORT A)

To accomplish the transfer of data, the data lines (D0-D7) of the PPI are connected directly to the lower 8 bits of the microprocessor data lines (AD0-AD7).

The read, write, and reset lines of the PPI are connected to same on the M80C186, while the A0 and A1 address pins of the PPI are connected to the PCS5/A1 and PCS6/A2 peripheral chip select/latched pins of the microprocessor. These PCS pins are software programmable and allow selection of the appropriate device. This connectivity allows the PPI to be programmed for device, control, and information flow. Since this is in software, it is easily modified, without major hardware wiring changes. In turn, the PPI can activate, program, and transmit/receive data from modules or peripherals down-line, based on software modifiable codewords received from the microprocessor.

3. Harris HCS245MS Tri-State Octal Transceiver

a. General Selection

The octal transceivers serve as two-way asynchronous bus drivers between the PPI and the command bus lines, buffering the data to all modules and incidently serving as a first level of protection between the PPI and anomalies from the command bus. Principle selection criteria of the HCS245MS (Figure 7) included:

1. Radiation tolerant
2. Aerospace class S screened
3. Low power design
4. High Current bus driver outputs

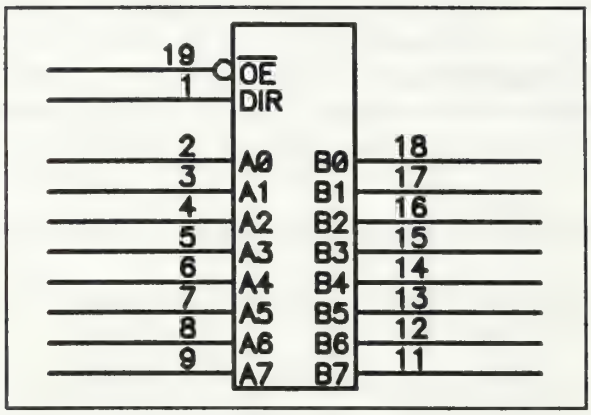

Figure 7 HCS245MS

b. Operation

Two HCS245MSs [Ref. 8: pp. 12-153 to 12-157] are required for the command bus interface design, one linked to the 8 pins of port A and the other to the 8 pins of port B. Since there are no devices on other modules capable of using port C lines to control port A data, port C control information currently does not require connectivity to the command bus. Because PPI port B is configured as output only, the transceiver connected to this port is hardwired as output only. Port A, however, is used for both input and output and so direction of the associated transceiver is controlled by pin PB7 of port B, the pin carrying the "read" command from the PPI.

C. MODULE COMMAND BUS INTERFACE

1. Harris HCS245MS Tri-state Octal Transceiver

Described in Section II.B.3, one of these devices, in concert with a 3-to-8 line decoder/demultiplexer, is used to decode the PPI address on each module. Operation of the module interface to the command bus is described in Section II.C.2.b.

Another transceiver is used as a bus driver for data between the module and the DCS command bus interface.

2. Harris HCS138MS CMOS/SOS Inverting 3-to-8 line Decoder/Demultiplexer

a. General Selection

A high-reliability, high-speed component, the HCS138MS [Ref. 8: pp. 12-57 to 12-61] of Figure 8 was selected based on:

1. Radiation hardened
2. Aerospace class S screened
3. Latch-up free under transient radiation

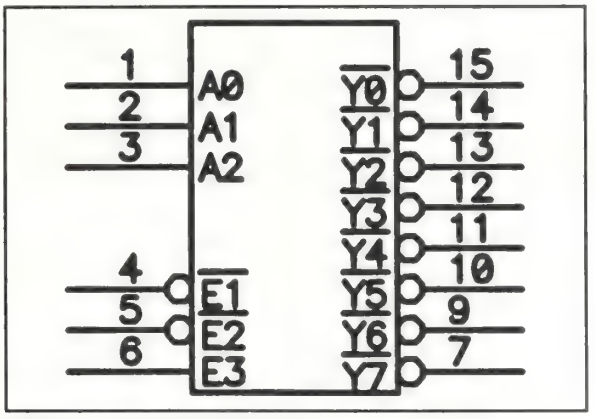

Figure 8 HCS138MS

b. Operation

This 3-to-8 line decoder/demultiplexer has outputs active in the low state and an associated truth table is provided in Table 2.5:

TABLE 2.5 DECODER/DEMULTIPLEXER TRUTH TABLE [REF.8: P. 12-57]

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

Used in conjunction with one of the octal transceivers, the decoder/demultiplexer is used to decode the PPI address of each module. This is accomplished with a circuit similar to Figure 9 (set for Mass Storage A decoder: PB3-PB0 = 0110).

As can be seen in Table 2.3, the PPI address of each duplicated module differs in only the PB3 bit. This means only the E1 and E3 lines of the 138 need to be switched and +5V changed to ground for each paired module to change the address.

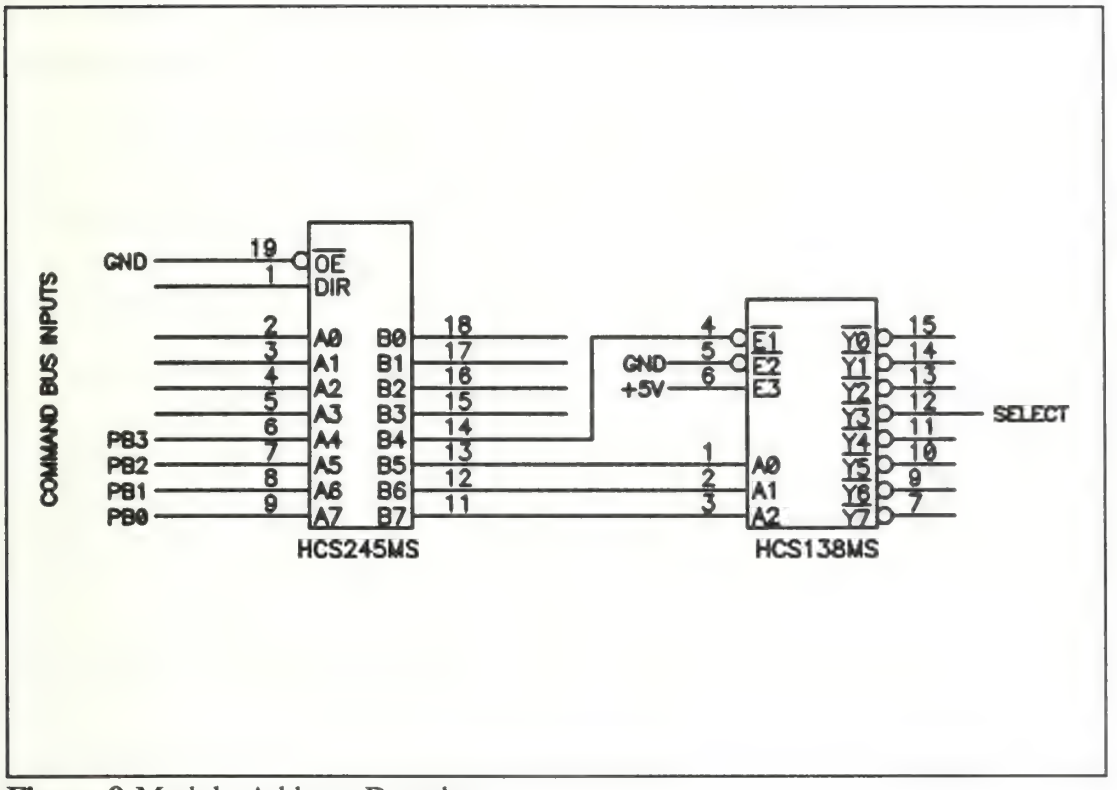

Figure 9 Module Address Decoder

III. SYSTEM MEMORY ARCHITECTURE

A. GENERAL

The DCS microprocessor has the capability of directly addressing up to 1 MByte of memory. With the exception of memory required for system read only memory (ROM) and random access memory (RAM), this space will be available as needed for other requirements system designers may have (eg. current telemetry, operating code, tables, etc). In addition to the 1 MByte of memory used by the DCS for system and operational requirements, an additional 4 MByte will be accessible in each of the mass storage areas, albeit at a much reduced access rate since use of the 8-bit command bus will be required. A PPI will be used to address memory in these modules. While specifically planned as "mailboxes" for satellite amateur radio operator users, these mass storage areas may also be used by the DCS as required.

The 1 MByte used by the DCS is broken into ROM, wherein resides the permanent storage for basic system activation, and RAM, to be used by the operating system as required. To generalize the design and allow for future modifications without significant hardware changes, the approach taken was to use 1 MByte of RAM overlaid by the required amount of ROM, a concept easily addressed in software and requiring only a minimal increase in hardware over using the microprocessor chip select features. This generalizes the design and allows for future selection of the amount of ROM required without impacting RAM placement or wiring.

Additionally, despite the inherent reliability of modern memory chips, due to the critical nature of system RAM, the decision was made to apply an error detection and correction (EDAC) capability to the 1 MByte of system memory aboard the DCS. An alternative would have been to duplicate the entire system memory section, a workable approach taken by Ashe [Ref. 5], but requiring a significant increase in wiring and space requirements over the EDAC method. Figure 10 is a map of system memory using the above approaches.

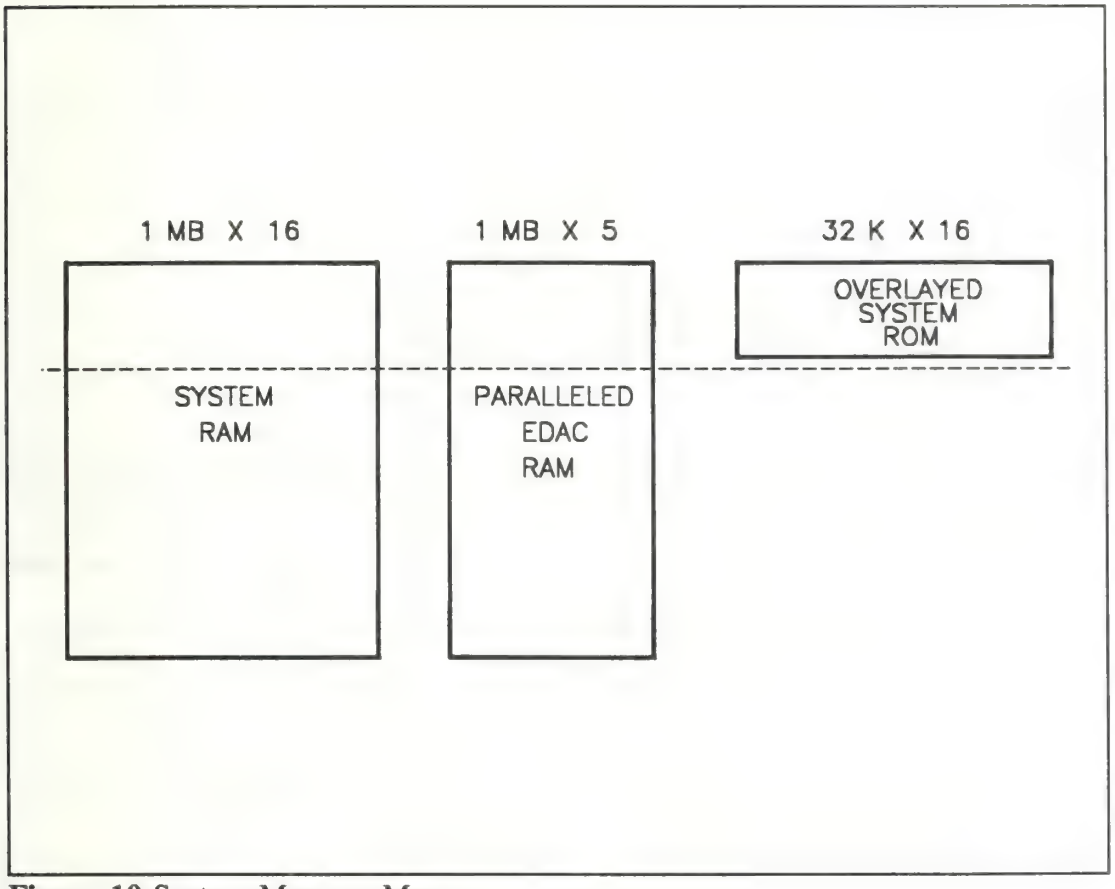

Figure 10 System Memory Map

B. SYSTEM MEMORY DESIGN

1. Texas Instruments TMS29F258-20NJQ4 Flash Electrically Erasable Programmable Read-Only Memory (EEPROM)

a. General selection

The EEPROM holds the basic programming required to activate the microprocessor aboard the DCS and system design calls for two of these chips per DCS. A number of memory devices are available which serve this function, and the TMS29F259-20 [Ref. 9: pp. 7-27 to 7-46] (Figure 11 germane) was selected for the following reasons:

1. Radiation tolerant
2. Low power design (max I_{cc} active: 15ma, max I_{cc} standby: 3ma)

b. Specific Features

A number of EEPROMs are suitable for PANSAT use and one of the advantages of this chip is that it adheres to the EEPROM JEDEC standard, making a pin for pin swapout with an alternative device feasible. The 32K X 8 Flash EEPROM operates at a relatively slow 200ns for maximum access time. The slow acces time is circumvented by reading the ROM into RAM immediately after the microprocessor has been activated to take advantage of the faster RAM access time.

Electrically programmable and erasable, the flash erase mode can be

activated by loading a dummy sequence of data and address strings as demonstrated in Table 3.1. After receiving this sequence, the self-timed flash mode starts automatically.

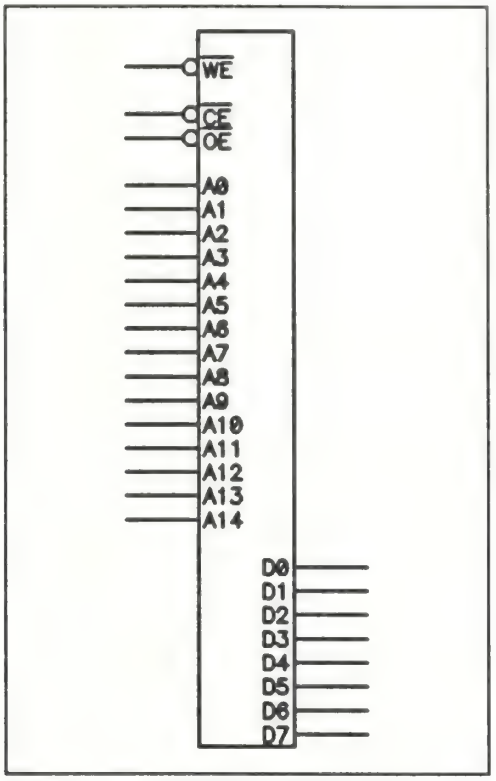

Figure 11 TMS29F258-20NJQ4

TABLE 3.1 FLASH ERASE MODE SEQUENCE

STEP	MODE	A14-A0	D7-D0
1	Access Write	5555	AA
2	Access Write	2AAA	55
3	Access Write	5555	80
4	Access Write	5555	AA
5	Access Write	2AAA	55
6	Access Write	5555	10

The EEPROM is also protected by hardware and software from inadvertent write commands.

c. Operation

Two of these devices are provided for DCS system memory. They use the chip select feature of the M80C186, coupled with the microprocessor signal for high or low word byte for chip activation, and are tied to the read and write lines of the microprocessor. The address lines are connected to the octal latches holding the address from the microprocessor while the data lines are connected directly to the address/data lines of the M80C186. Implementation of this design is demonstrated in Figure 12. Because of the overall design of system memory and the overlapping of ROM onto RAM, RAM addressing is covered in section B.2. These ROM chips may be easily swapped pin-for-pin with larger or smaller ROM chips without affecting the addressing scheme or RAM memory map, other than minor changes to software.

2. Mosaic MSM8128JLMB-85 128K X 8 Static RAM (SRAM)

a. General Selection

As with ROM, a number of different SRAM chips are possible. The MSM8128JLMB-85 [Ref. 10: pp. 2-79 to 2-88] (Figure 13) was selected based principally on:

1. high speed (85ns)
2. low power (standby: 10 microwatt (typ), active: 75mW (typ))
3. available in MIL-STD-883 grade

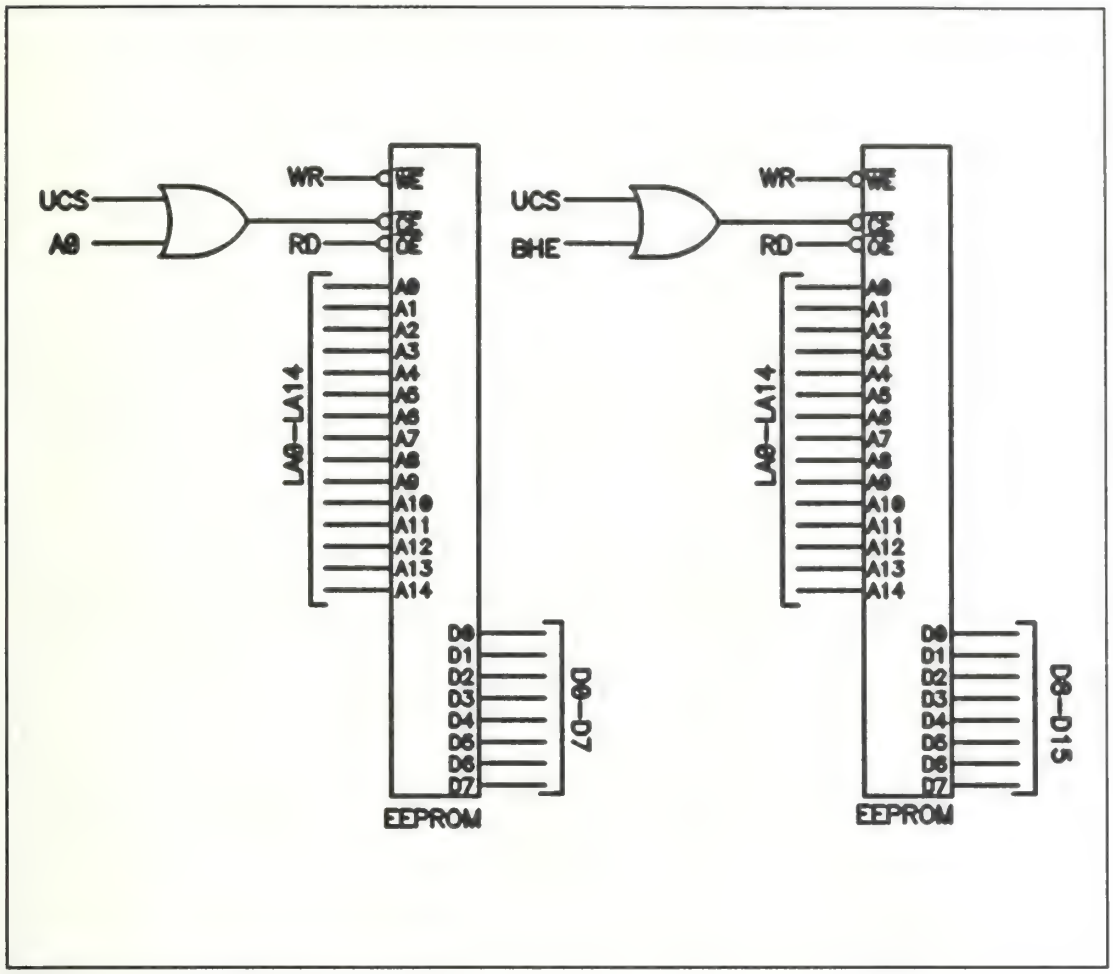

Figure 12 ROM Addressing

b. Operation

Eight of these memory chips are required for the 1 MByte of DCS system memory (less ROM). They are addressed by means of a dual 2-to-4 line decoder/demultiplexer which allows selection of the chips without using the chip select features of the microprocessor, and thereby implements the mechanism by which ROM memory mapping overlays RAM. Selection of the individual chip for activation keys on the last two bits of the address provided by the microprocessor (AD18-AD19) and whether a high or low byte, or both, is being written to or read from.

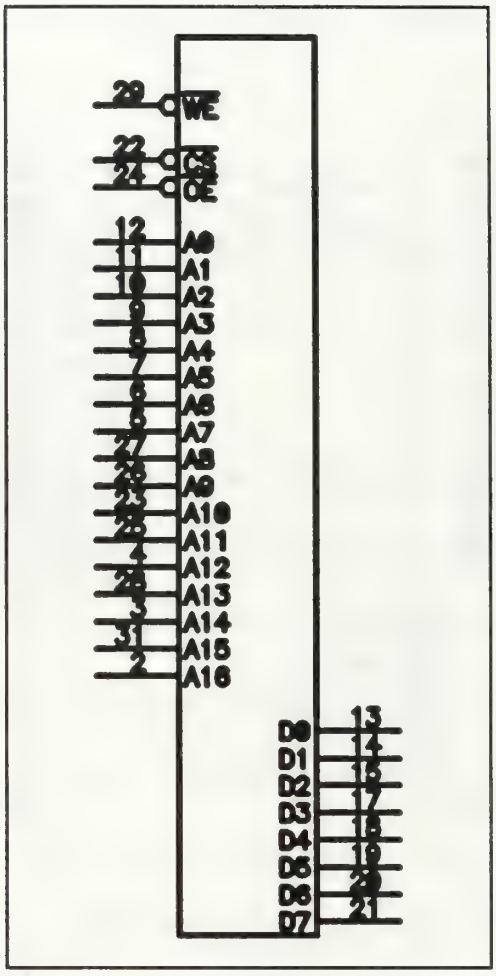

Figure 13 MSM8128JLMB-85

An inhibitor to the chip enabling process is whether the UCS (upper chip select) has been selected by the microprocessor. If UCS is active, then the SRAM is not enabled and the ROM is. This is the mechanism which allows ROM to effectively be mapped onto RAM, with the addresses included in UCS being determined by software (see figure 14). In this way, an entire MByte of SRAM is available, less the amount finally determined to be required by ROM.

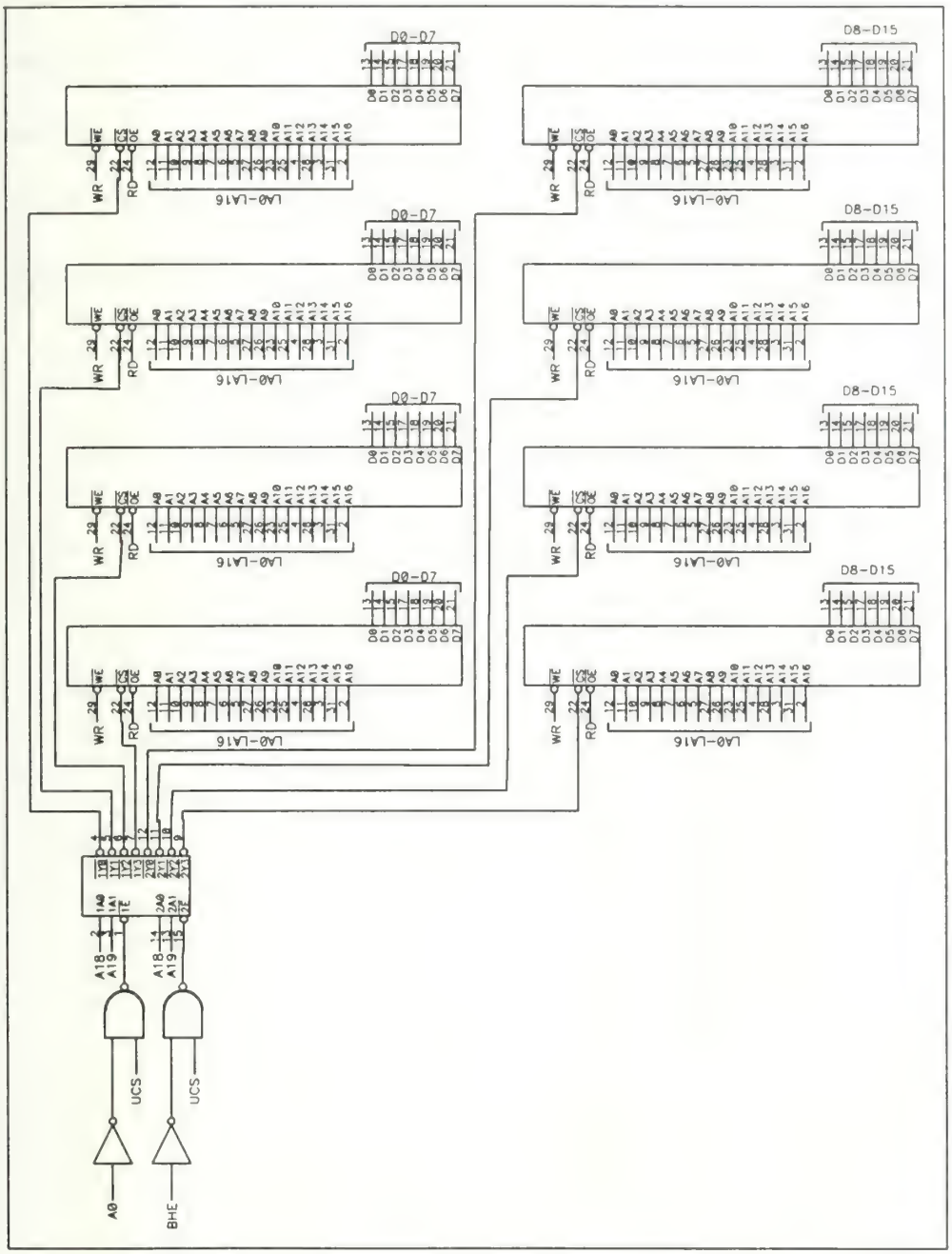

Figure 14 RAM Select Process

3. Electronic Designs EDI84256CS 256K X 4 SRAM

a. General Selection

Again, a number of suitable memory chips are available and may be swapped for the EDI84256CS [Ref. 11: pp.329-334], Figure 15, pin-for-pin if desired. Principle selection criteria:

1. High speed (55ns)
2. Low power (standby: 20 mA max, active: 180 mA max)
3. Available in MIL-STD-883 grade

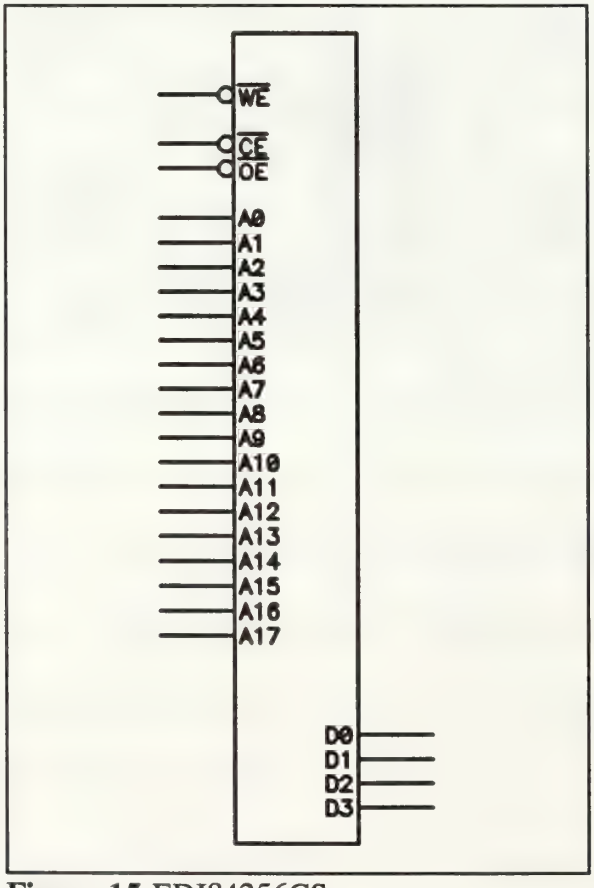

Figure 15 EDI84256CS

b. Operation

Four of these chips are required for system memory and they are dedicated to EDAC use, storing the first 4 bits of the 5-bit EDAC check bits generated for each 8-bit word. Like the 128K X 8 SRAM chips used to store system memory, chip selection is keyed through use of address and control lines from the microprocessor as determined by a decoder/demultiplexer. Since these chips are 256K X 4, however, the chip enable function is activated by an "or" of two of the output lines from the decoder/demultiplexer, as demonstrated for one chip in Figure 16.

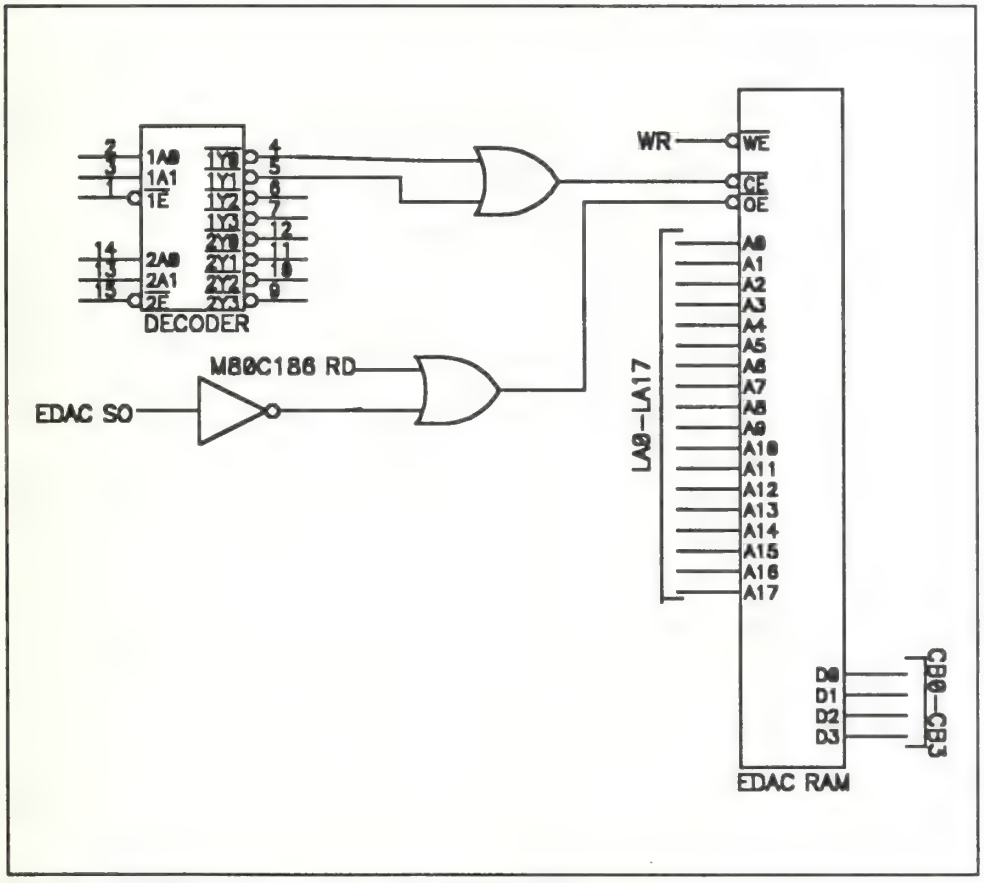

Figure 16 EDAC Syndrome RAM Select

4. Electronic Designs EDI81256C 256K X 1 SRAM

a. General Selection

Interchangeable with similar memory if so desired, the EDI81256C [Ref. 11: pp. 293-298] (Figure 17) was selected for the following reasons:

1. high speed (55ns)
2. low power (standby: 20 mA max, active: 120 mA max)
3. available in MIL-STD-883 grade

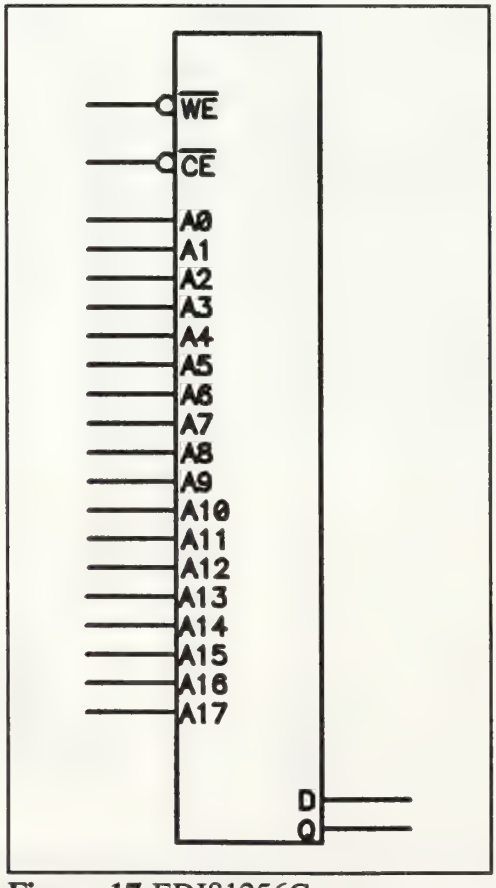

Figure 17 EDI81256C

b. Operation

The four of these chips required for DCS memory are used to store the fifth bit of the checkword generated by the EDAC process (each chip is paired with an EDI84256CS). Selection of these chips is identical to that of the EDI84256CS of Section III.B.3 and connectivity is similar to Figure 16.

5. Harris ACS630MS Error Detection and Correction Circuit (EDAC)

a. General Selection

To avoid the construction of a dual memory section and associated hardware to toggle between the sections, and yet ensure reliable memory, an EDAC circuit was incorporated into the PANSAT DCS system memory design. The ACS630MS [Ref. 12: pp.7-56 to 7-63] (Figure 18) was selected based on the following criteria:

1. Radiation hardened
2. Available in MIL-STD-883 grade
3. Low power consumption
4. Latch-up free under any conditions

b. Operations

The EDAC chip selected for PANSAT operations is a 16-bit parallel error detection and correction circuit. It operates on the principle of single-bit correct and double bit detect. In other words, if only one bit in a word is detected in error the EDAC chip pinpoints the incorrect bit based on the 6-bit error syndrome code generated

when the word is initially written to memory, flips the bit, and releases the corrected word while setting a single error flag (SEF). If a single error is noted in the checkword the single error flag is set but no corrections are made.

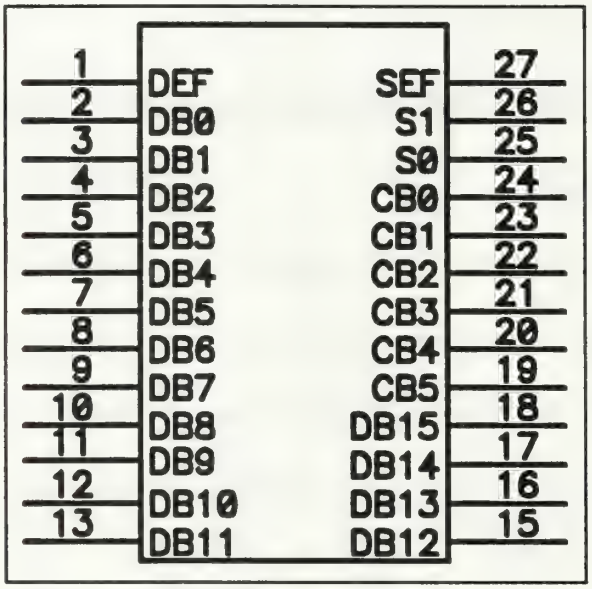

Figure 18 ACS630MS

In both cases, the single error flag can be used to generate an interrupt in the microprocessor, making it possible to accumulate and analyze possible patterns in error development related to radiation or component aging. If two bits are noted in error, a double error flag (DEF) is set which can be used to generate a hard interrupt for the microprocessor.

Two of these chips are required for the system RAM since, as Clements [Ref. 13: p. 463] so eloquently states, "The most irritating problem associated with codes for error detection/correction is due to the modern 16-bit processors's ability to operate on a whole 16-bit word or just 1 byte of it." When the M80C186 writes or reads

to memory, it has the option of using the entire 16-bit word or just the lower or upper 8 bits. This leads to complications with respect to memory manipulation for EDAC processing when only 8 bits are used.

Using a single 16-bit EDAC chip with a microprocessor capable of byte operations necessitates a complicated memory control structure to ensure that check bits are associated with the correct corresponding memory locations. For example, with 6 bits of check bit storage per 16-bit word, if the microprocessor writes only the upper or lower byte, then:

1. the current 16-bit word in memory location must be made available on the bus
2. the byte being written to must be replaced by the new data
3. the check bits on the entire 16-bit word must be generated and stored
4. the new byte must be stored in memory

Similarly, if the microprocessor reads only one byte, the entire associated 16-bit word and its attendant 6 check bits must be made available on the bus to the microprocessor and checked for error before releasing the byte to the microprocessor. Both of these situations require additional time and read operations in excess of that required by the EDAC circuit for standard operations.

The method chosen to avoid the complicated memory control circuitry and time penalties of the 16-bit EDAC was to use two 8-bit EDAC circuits. The penalty for this approach was the addition of one EDAC chip and two additional 256K X 4 memory chips to the design, since 5 bits are required to generate check bits per byte of data and retain the single bit correct/double bit detect function. A review of available

board space indicated this approach was feasible and had the added advantage of eliminating several potential failure points which would have been introduced by additional memory control circuitry.

EDAC operation is relatively simplistic in that only two control lines, S0 and S1 (Figure 18 germane), are required to accomplish the one write and three read functions of the unit. Table 3.2 summarizes control functions:

TABLE 3.2 EDAC CONTROL FUNCTIONS

Memory Cycle	Control		EDAC Function	Data I/O	Error Flags	
	S1	S0			SEF	DEF
Write	Low	Low	Generate checkword	Input data	Low	Low
Read	Low	High	Read data and checkword	Input data	Low	Low
Read	High	High	Latch and flag error	Latch data	enable	enable
Read	High	Low	Correct data word and generate syndrome	Output corrected data	enable	enable

The EDAC chip uses a modified Hamming code based on a 16-bit data word to generate 6 check bits. With only 8-bit data being processed by the EDAC chip, the other data lines are tied low to supply zeros to check bit generation and the fifth check bit is not required. This bit is also tied low since the check bit pins are used to input the generated syndrome from memory for error detection and correction. Table

3.3 demonstrates that the six check bits (CB0-CB5) are parity bits derived from the matrix of indicated data bits.

TABLE 3.3 EDAC CHECKWORD GENERATION [Ref. 12: p. 7-57]

CHECKWORD BIT	16-BIT DATA WORD															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

The M80C186 has programmable wait states selectable for memory operations. Based on timing diagrams of the microprocessor and components involved, use of the EDAC circuitry should required no more than 1 wait state inserted at the appropriate location (T_3). Should slower memory be selected or other design modifications slow memory operations, up to three wait states can be implemented without resorting to external circuitry. The EDAC hardware was designed to make it easy to add delays to the EDAC, should this be required, by simply adding additional lines from the line decoder/demultiplexer to the NAND gate controlling S0. The EDAC circuit is demonstrated in Figure 19.

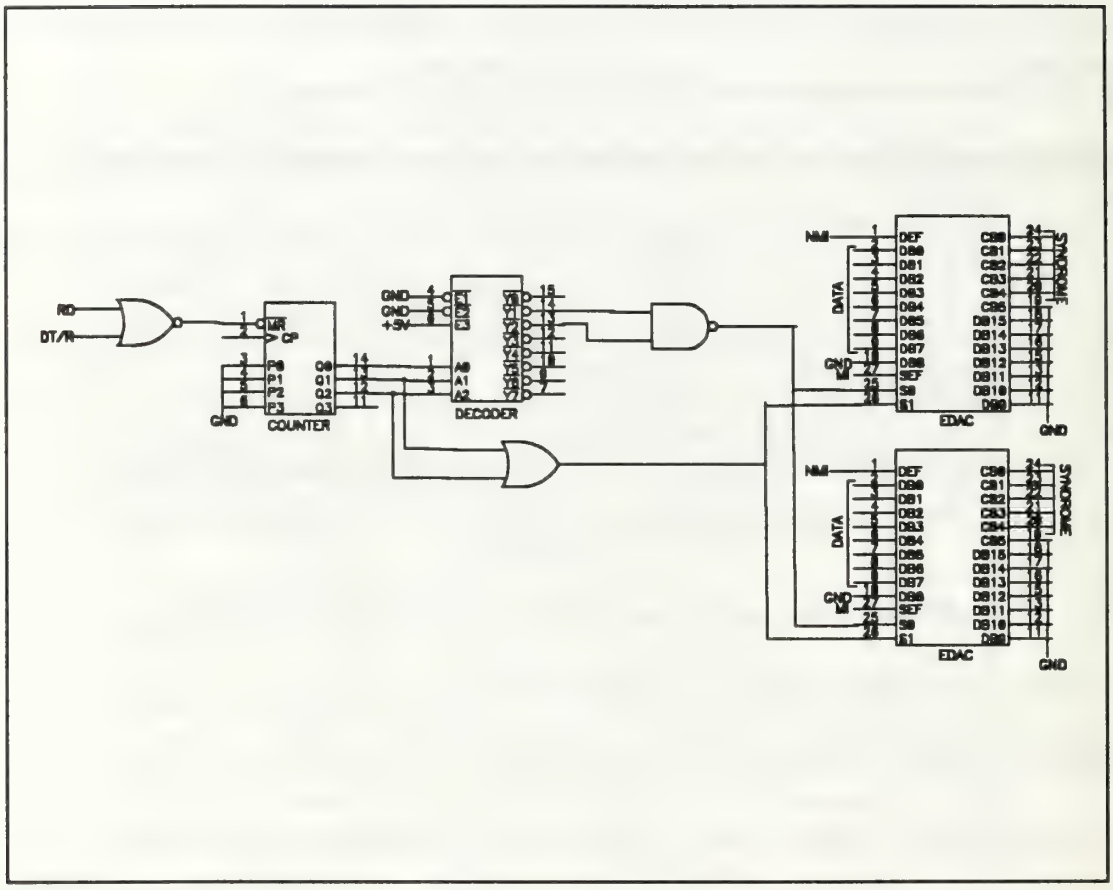

Figure 19 EDAC Circuit

6. Harris HCS138MS 3-to-8 Line Decoder/Demultiplexer

Described in Section II.C.2, this device is used to select the values of one of the EDAC control bits, S0, based on input from a counter which cycles the required EDAC control pattern. Table 3.2 shows the required sequence of control bits (S0, S1) for write and read operations.

7. Harris HCS161MS CMOS/SOS Presettable 4-bit Binary Counter with Asynchronous Reset

a. General Selection

This HCS161MS [Ref. 8: pp. 12-91 to 12-95] high reliability, high speed counter, shown in Figure 20, has the following desirable characteristics:

1. Aerospace Class S screened
2. Radiation hardened
3. Latch-up free under transient radiation
4. High speed

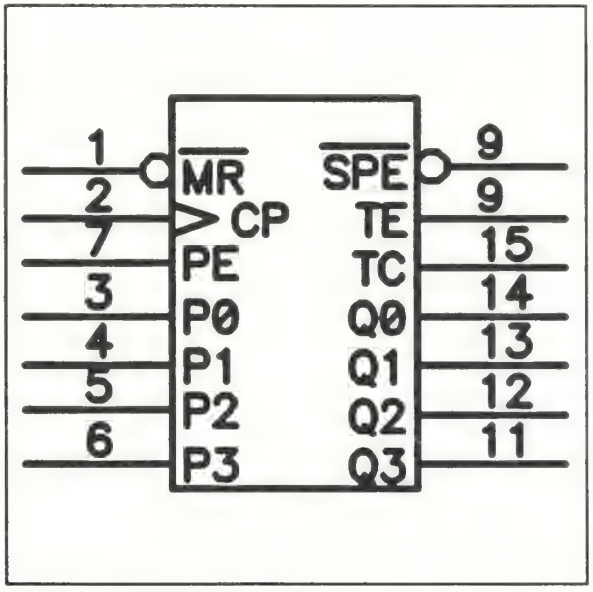

Figure 20 HCS161MS

b. Operation

It is only necessary to use the lower three bits of the HCS161MS counter to drive the decoder/demultiplexer since this provides more than enough cycles (eight)

to operate the EDAC chip (depending on memory speed, EDAC should only require four cycles). Outputs are kept low until a memory read is required, then the counter is used in conjunction with the decoder/demultiplexer to generate control bits for EDAC operation (Figure 19 germane).

8. Harris HCS27MS Triple 3-input NOR Gate

The HCS27MS [Ref. 8: pp. 12-6 to 12-11], shown in Figure 21, is used in the EDAC control circuitry to determine when to initiate the counter and also in the SRAM selection process to enable the individual decoders for the memory banks selected by the dual 2-to-4 line decoder/demultiplexer. It was selected based on:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

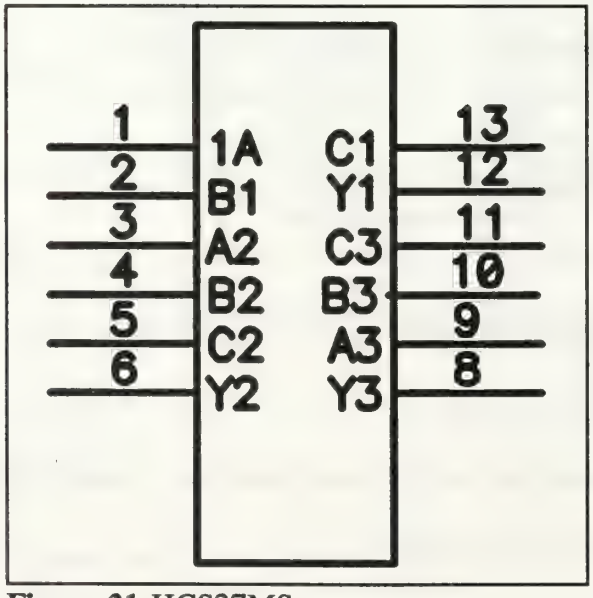

Figure 21 HCS27MS

9. Harris HCS00MS Quad 2-input NAND Gate

The HCS00MS [Ref. 8: pp. 12-6 to 12-11] shown in Figure 22 is used in EDAC control circuitry for selecting input to the S0 control line. It was selected based on:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

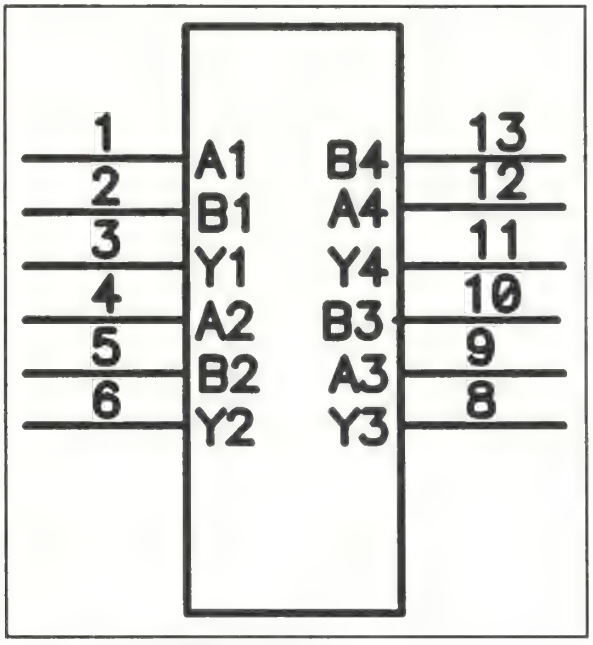

Figure 22 HCS00MS

10. Harris HCS32MS Quad 2-input OR Gate

The HCS32MS [Ref. 8: pp. 12-6 to 12-11] is used in the EDAC control circuitry for selecting the signal for the S1 control line. Shown in Figure 23, it was selected due to:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

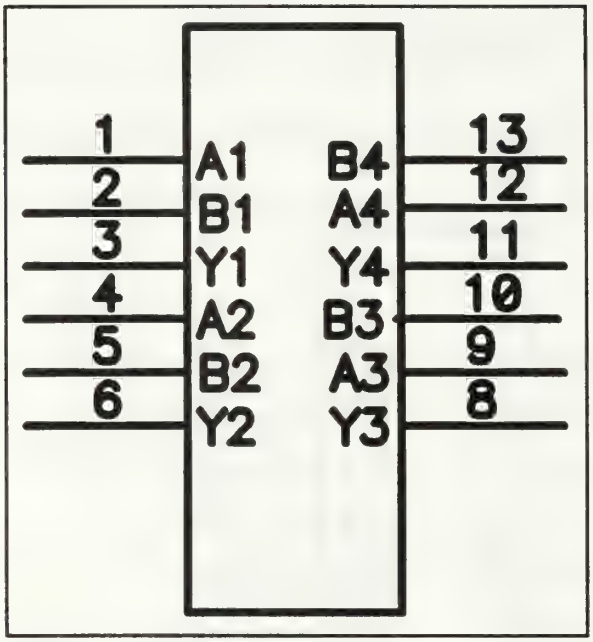

Figure 23 HCS32MS

11. Harris HCTS139MS Dual 2-to-4 Line Decoder/Demultiplexer

a. General Selection

The dual 2-to-4 line decoder serves as the chip enable selector for the SRAM of system memory. The HCTS139MS [Ref. 8: pp. 12-67 to 12-70] presented in Figure 24 was selected to fill this critical single point of failure position. Loss of this

chip would deny access to system SRAM aboard a DCS rendering the module useless. The device was selected based on the following criteria:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High reliability
5. High speed

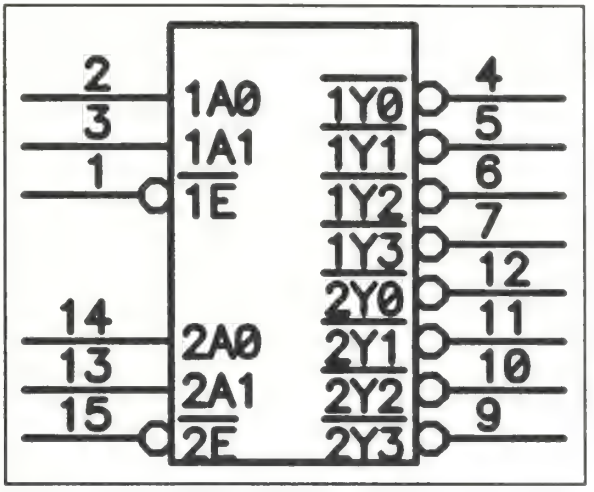

Figure 24 HCTS139MS

b. Operation

Only one of these components is required to access SRAM. Each decoder/demultiplexer in the dual package is used to access one bank of memory based on high or low byte write/read from the microprocessor. The last two digits of the address, A18 and A19, are used to select the individual chip within the high or low bank of memory (Figure 14 germane). The enable function of each decoder/demultiplexer is tied to selection of the bank (high: BHE line of microprocessor, low: LA0 or latched

A0 line of microprocessor) and the upper chip select (UCS) of the microprocessor which is the mechanism used to differentiate between ROM and SRAM addresses. Tables 3.4 and 3.5 provide the truth tables used to select individual memory chips (decoder/demultiplexer is enabled low) while Figure 25 demonstrates implementation of the HCTS139MS.

TABLE 3.4 DECODER 1 TRUTH TABLE

INPUT					OUTPUT			
LA0	**UCS**	**E**	**A19**	**A18**	**Y3**	**Y2**	**Y1**	**Y0**
0	0	1	X	X	1	1	1	1
1	0	1	X	X	1	1	1	1
1	1	1	X	X	1	1	1	1
0	1	0	0	0	1	1	1	0
			0	1	1	1	0	1
			1	0	1	0	1	1
			1	1	0	1	1	1

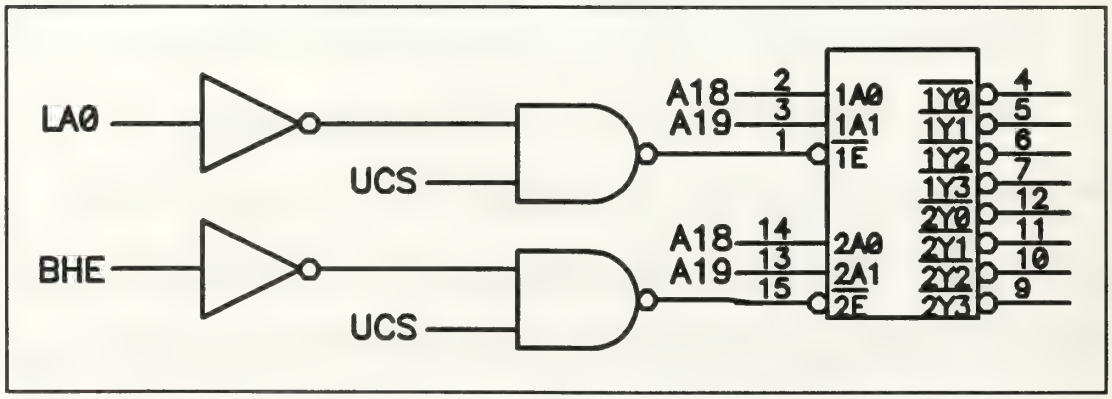

Figure 25 RAM Decoder Implementation

TABLE 3.5 DECODER 2 TRUTH TABLE

INPUT					OUTPUT			
BHE	**UCS**	**E**	**A19**	**A18**	**Y3**	**Y2**	**Y1**	**Y0**
0	0	1	X	X	1	1	1	1
1	0	1	X	X	1	1	1	1
1	1	1	X	X	1	1	1	1
0	1	0	0	0	1	1	1	0
			0	1	1	1	0	1
			1	0	1	0	1	1
			1	1	0	1	1	1

12. Harris HCS245MS Tri-state Octal Transceiver

Described in Section II.B.3, two of these devices are used to prevent overloading of the microprocessor by buffering the data output from pins AD0-AD15. The direction of the data flow is determined by the DT/R (Data Transmit/Receive) output of the microprocessor, while the device is enabled for I/O associated with system SRAM, the serial communications controller, the programmable interval timer, the A/D Converter, or Spread Spectrum control. This enabling is accomplished by use of the active peripheral chip select pin of the M80C186 (Table 2.1 germane).

A truth table of device operation is presented in Table 3.6 while the associated hardware connectivity is demonstrated in Figure 26.

TABLE 3.6 TRANSCEIVER TRUTH TABLE

S0	UCS	PCS0	PCS1	PCS3	PCS4	ENABLE
0	0	X	X	X	X	1
0	1	X	X	X	X	0
1	0	X	X	X	X	1
1	1	X	X	X	X	1
X	X	0	X	X	X	0
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0

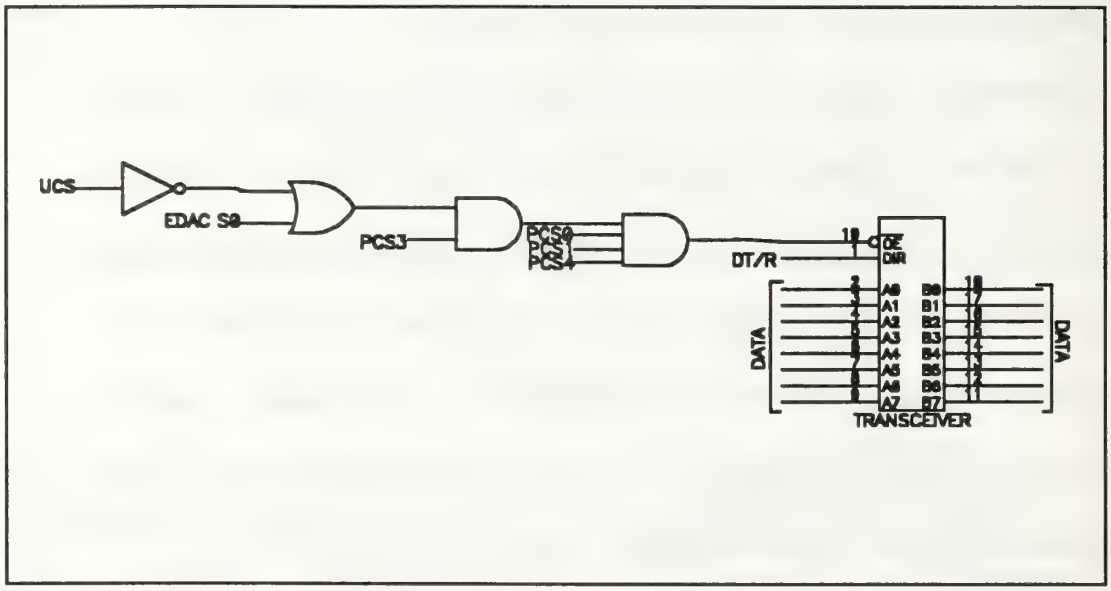

Figure 26 Transceiver Connectivity

13. Harris HCTS21MS Dual 4-input AND Gate

The HCTS21MS [Ref. 8: pp.12-12 to 12-19] is used to determine enabling of the octal transceiver buffering the data between the microprocessor and selected peripherals. Shown in Figure 27, selection criteria include:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

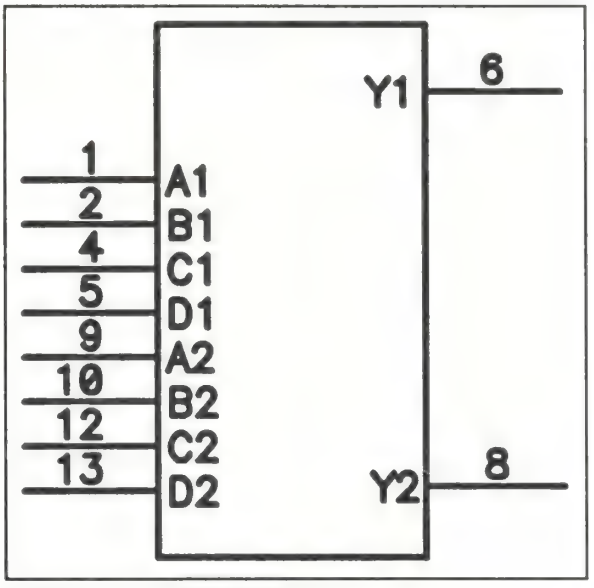

Figure 27 HCTS21MS

14. Harris HCS04MS Hex Inverter

Three inverters are required in implementing the memory decoder section of the DCS as designed. The HCS04MS [Ref. 8: pp. 12-6 to 12-10], as shown in Figure 28, was selected based on the following criteria:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

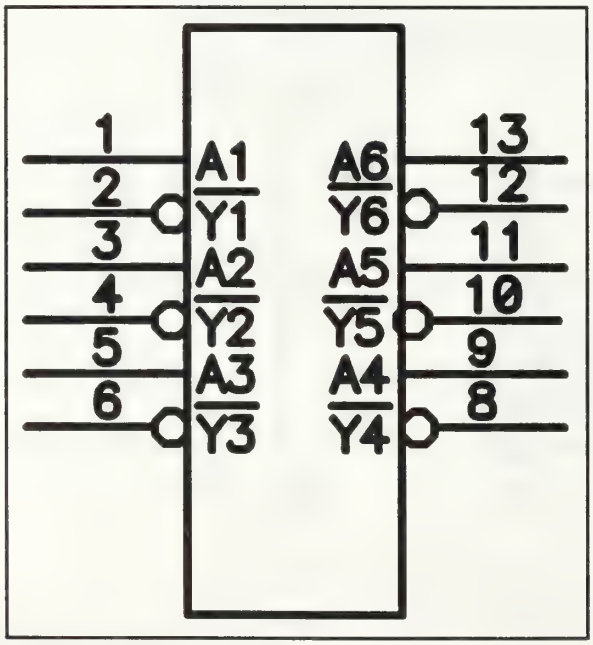

Figure 28 HCS04MS

15. Harris HCS573MS Octal Transparent Latch

Three HCS573MS devices [Ref. 8: pp. 12-202 to 12-206] are used to latch the 20 address lines (AD0-AD19) and the BHE (bus high enable) line from the microprocessor. Since the Address/Data bus is time multiplexed, the address data must

either be latched internally by a specific peripheral or by these external latches. The three devices are implemented in parallel to ensure the address information is stable and available as required. The output enable pin of the latches is tied low, constantly enabling output, since the high impedance state is not required. The latch enable pin, active low, is tied to the address latch enable (ALE) pin of the microprocessor which is provided for this purpose. The ALE goes high when the address data is available on the bus, then goes low, enabling the latch of the HCS573MS, while the address information is still valid and before the A/D bus of the microprocessor provides data. Shown in Figure 29, the device was selected based on:

1. Radiation hardened
2. Aerospace Class S screened
3. Latch-up free under transient radiation
4. High speed

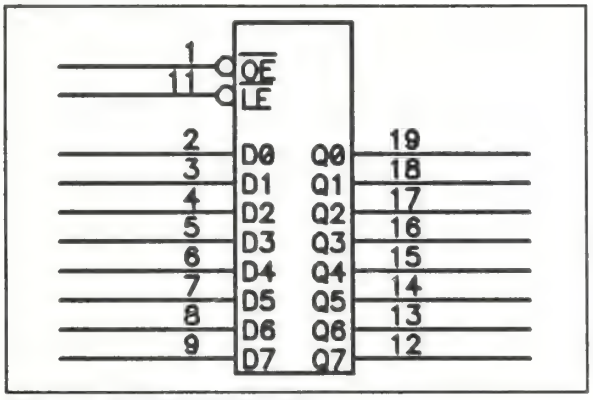

Figure 29 HCS573MS

IV. SENSOR ANALOG-TO-DIGITAL CONVERSION

A. GENERAL

PANSAT has a number of telemetry collection requirements that must be satisfied (e.g. temperature, current, voltage, etc) in order to determine the physical operational status of various spacecraft systems, and a means had to be devised to convert the analog signals derived from these devices into digital form for processing by the M80C186. Insofar as design of this portion of the DCS is concerned, it is sufficient to know that the analog to digital conversion requirement exists since a system can be designed to convert the sensor analog signals to digital by treating the analog side of the circuit as a black box. Because of the modular design of PANSAT components, Analog multiplexers A and B (Figure 1) are the black boxes containing the analog processing circuitry. Although power and control lines for these modules are carried on the command bus, there is direct connectivity between the 4 channel multiplexer of the ADC (analog-to-digital converter) and both mux modules used for the receipt of data. As shown in Figure 1, the PANSAT block diagram, this is one of only two instances where the command bus is not used exclusively (the other being between DCS and the RF system).

The approach taken for this part of the DCS was to design an interface with sufficient capability to process anticipated analog input. In point of fact, Horning and Sheltry [Ref. 14] put forth a comprehensive design of the analog circuitry necessary to provide input to the ADC.

B. DESIGN

1. Requirements

A requirement for in excess of 40 sensors currently exists. Table 4.1 contains an anticipated list of sensors. Associated range values are provided where known to date.

TABLE 4.1 SATELLITE ON-BOARD TELEMETRY REQUIREMENTS

SENSOR	NOMINAL		OPERATIONAL	
	MIN	MAX	MIN	MAX
(17) SOLAR ARRAY TEMP (°C)	0	50	-20	120
(2) BATTERY VOLTAGE (V)	12	13	11.5	13.5
(4) BATTERY TEMP (°C)	-1.1	10	-6.7	26.7
(2) BATTERY DISCHARGE CURRENT	TBD	TBD	TBD	TBD
(1) EPS BUS VOLTAGE	TBD	TBD	TBD	TBD
(2) EPS BOARD TEMP (°C)	0	40	-10	50
(1) TRANSMITTER CURRENT	TBD	TBD	TBD	TBD
(2) TRANSMITTER RF POWER	TBD	TBD	TBD	TBD
(2) RECEIVED SIGNAL STRENGTH	TBD	TBD	TBD	TBD
(2) RECEIVER TEMP (°C)	0	40	-10	50
(2) TRANSMITTER TEMP (°C)	0	40	-10	50
SENSE RELAYS FOR COMMS HARDWARE	TBD	TBD	TBD	TBD

SENSOR	NOMINAL		OPERATIONAL	
	MIN	MAX	MIN	MAX
(2) DCS BOARD TEMP (°C)	0	40	-10	50

The ADC must be capable of easy microprocessor interface to allow transfer of data, addressing and control information. An internal clock with reference and internal sample and hold capability is desirable. Additionally, a minimum of 12-bit resolution and programmable gain are required, along with overflow detection.

2. National Semiconductor LM12H454 12 Bit Plus Sign Data Acquisition System with Self Calibration

a. General Selection

The LM12H454 [Ref. 15], shown in Figure 30, satisfies all requirements cited in the preceding section, and additionally has the following desirable features:

1. Available in MIL-STD-883 grade
2. 4-channel multiplexer
3. Expansive microprocessor interface
4. Operates on single +5V power supply
5. Low power
6. 16-bit parallel I/O

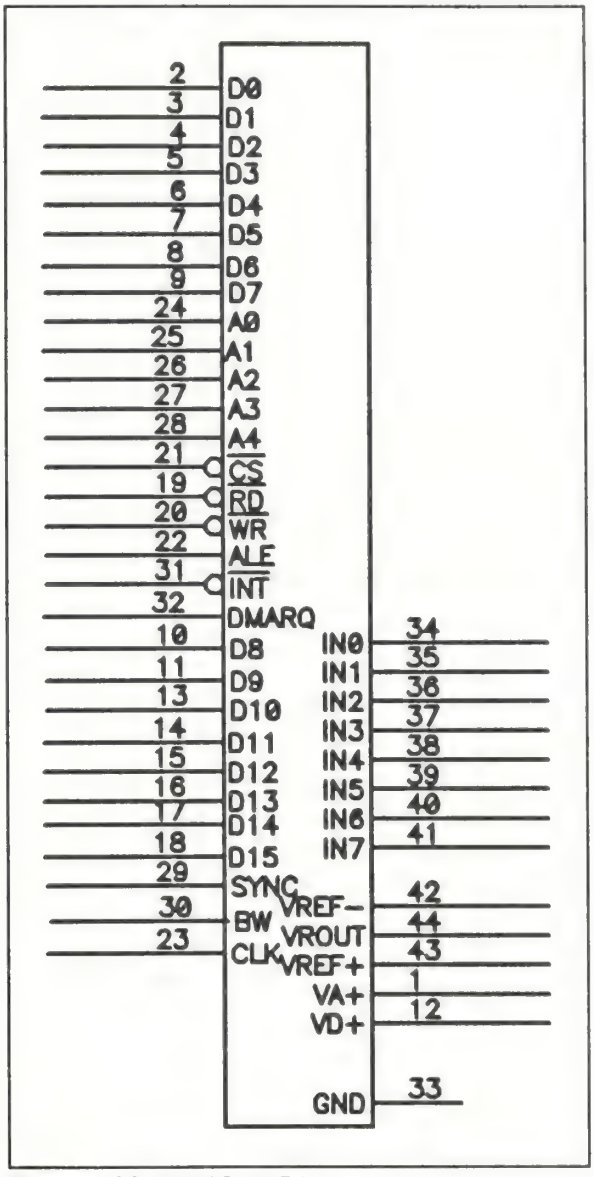

Figure 30 LM12H454

b. Additional Features

This device contains a fully differential and self calibrating 13-bit (12-bit and sign) analog-to-digital converter and a four-channel analog multiplexer. A 16-bit wide, 32-word, first-in-first-out (FIFO) data buffer can store up to 32 consecutive conversions. This reduces microprocessor overhead by allowing the M80C186 to wait for an interrupt, generated any time a specific number of conversions (up to 32) is completed, before reading the device or to read the FIFO buffer for stored conversions at any time. The internal clock driver timers allow programmable conversion sequencing and acquisition times. A direct memory access interface is provided and all registers, RAM, and the data buffer can be addressed through the microprocessor interface. A functional diagram is provided in Figure 31.

The LM12H454 has three modes of operation:

1. 12-bit plus sign with correction
2. 8-bit plus sign without correction
3. 8-bit plus sign comparison ("watchdog")

Mode 3, the supervisory or "watchdog" mode, provides two limits per sampled signal and can generate an interrupt if inputs are between or outside the set limits (software selectable). After one of these interrupts, the microprocessor could generate a conversion command and read the magnitude of the signal.

Two internal calibration modes are available, an abbreviated mode for correcting offset voltage alone, and a more comprehensive mode correcting both offset voltage and linearity error. Additionally, a 2.5V reference output is provided as a virtual ground for telemetry analog conditioning circuits. This device also has the capability to support additional analog signal processing by providing signals to external circuits.

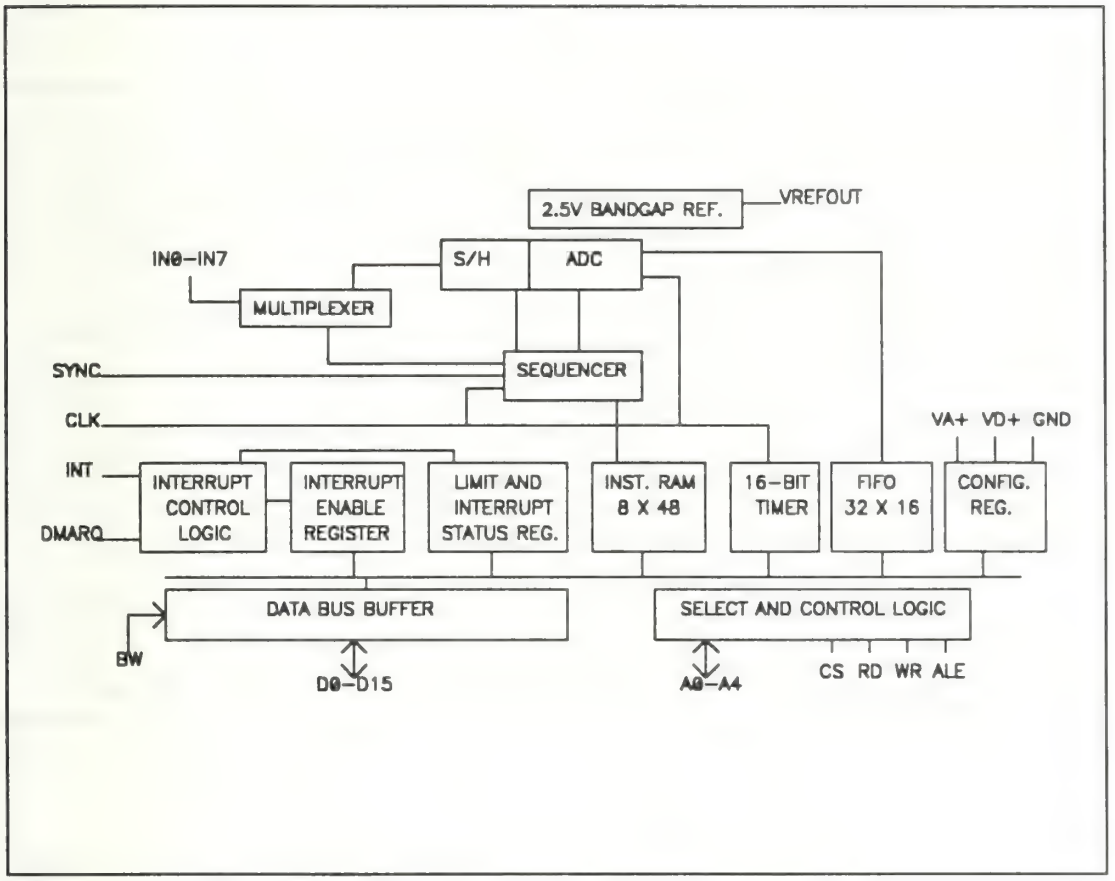

Figure 31 ADC Functional Diagram

However, this requirement is not anticipated and the associated pins (MUXOUT/ S/H) will be tied off as required.

c. Registers

A number of internal user-programmable registers provide flexibility in operations. The instruction RAM holds up to 8 sequentially executable instructions and is divided into three, 16-bit, individually addressable sections (8 X 48). These instructions can include multiplexer channel selection (to include acquisition time and resolution), "watchdog" limits and interrupt generation information, synchronization requirements, timing and conversion resolution.

The configuration register is a 16-bit control register used to hold general information along with calibration, reset and standby commands, while the timer register holds the user defined timing value which is used to delay the execution of instructions or slow the conversion rate.

The interrupt status register holds one of eight possible interrupts, all with the same priority unless masked, accessible to the microprocessor (Table 4.2 germane). Upon receiving an interrupt from the ADC, the microprocessor can read the interrupt status register to determine the type of interrupt which was generated and initiate appropriate action.

This register also holds the current number of conversions stored in the conversion register and the address of the instruction being executed. The associated interrupt enable register is programmed to enable the interrupts available to the ADC.

The limit status register (read only) is set whenever the input voltage of an instruction exceeds the preset limits and holds the status of the two limits for each of the eight instructions.

TABLE 4.2 ADC INTERRUPTS

NO.	INTERRUPT
0	ANALOG INPUT VOLTAGE OUTSIDE/INSIDE SPECIFIED LIMITS
1	INSTRUCTION COUNTER VALUE HAS BEEN REACHED (BUT NOT EXECUTED
2	CONVERSION REGISTER HAS REACHED PROGRAMMED NUMBER OF CONVERSIONS
3	COMPLETION OF ABBREVIATED CALIBRATION
4	COMPLETION OF FULL CALIBRATION
5	INSTRUCTION WITH A "PAUSE" BIT SET HAS BEEN REACHED
6	LM12H454 POWER SUPPLY VOLTAGE DROPS BELOW 4V (POTENTIAL FOR CORRUPTED DATA)
7	ISSUED AFTER RETURN FROM STANDBY TO ACTIVE MODE TO ALLOW CIRCUITS TIME TO SETTLE

The conversion register has thirty two 16-bit wide locations for holding the 12 bits of conversion data and the sign bit, along with the instruction address that generated the conversion. If more than 32 conversions are loaded without being read out, the oldest data is lost.

d. Connectivity

The 16 data pins of the ADC (D0-D15) are connected to the two tri-state octal transceivers (Section III.B.12 and Table 3.6 germane) buffering the output of the 16 data pins (AD0-AD15) of the microprocessor. The associated bus width input pin (BW) of the ADC is tied low to set the bus width to 16-bits.

The ADC address pins (A0-A4) are used to access all internal registers. These are tied to the octal transparent latch (Section III.B.15 germane) used to latch the least significant address bits from the microprocessor.

The read (RD), write (WR), and address latch enable (ALE) pins of the ADC are all tied to the associated pins of the microprocessor.

The ADC is capable of operating at clock speeds from 0.05 MHz to 10 MHz. Thus, the CLK pin of the ADC is connected directly to the CLKOUT pin of the 10 MHz microprocessor, a connection that will have to be adjusted should a faster microprocessor be selected.

The interrupt pin (INT) of the ADC is tied to one of the four maskable interrupt pins of the microprocessor by way of an inverter, since the interrupt signal from the ADC is active low and the interrupt inputs of the microprocessor are active high.

On receiving an interrupt signal from the ADC, the microprocessor can then read the interrupt status register to determine the type of interrupt which was generated.

ADC DMARQ (direct memory access request) is tied directly to the DRQ1 pin of the microprocessor when a transfer is ready to be performed.

There are four analog signal inputs to the multiplexer (IN0-IN3) which are selected through instruction RAM. Depending on final design requirements, these can be configured as four single-ended inputs or any two can operate as a differential pair. Multiplexer inputs will be tied directly to the analog mux modules and some flexibility in design exists at this point. Since each DCS must be able to access the four analog inputs from each analog mux module, one possibility is to gate the eight input lines and use one of the excess control lines from the command bus control interface PPI (Table 2.4 germane) to select the active mux module signals to be processed by the ADC. An alternative, allowing greater redundancy but at the cost of increased board space and somewhat increased power consumption, is to use duplicate ADCs, one for each set of four input lines from the mux modules, with the active ADC selected by the excess PPI control line.

Further hardware connectivity and software programming is dependent upon system sensor selection and operation.

V. COMMUNICATIONS

A. GENERAL

The primary function of PANSAT is to communicate with amateur radio stations around the world using half-duplex spread spectrum communications with the asynchronous data transfer protocol AX.25, currently in wide use by amateur radio operators for packet communications. As currently envisioned, in addition to the command bus interface, each DCS will also have direct connectivity with the RF section (Figure 1, PANSAT block diagram germane). All communications signal processing will take place in the communications section of each DCS.

B. DESIGN

1. Limitations

No fully-implementable design is provided for this segment of DCS. An existing requirement to incorporate a one-chip solution for a spread spectrum receiver in an Application Specific Integrated Circuit (ASIC) device, the PARAMAX PA-100 Spread Spectrum Demodulator [Ref. 16], was a limiting factor in this area. Full technical data on the 223 pin device was not received in time to incorporate it into a functional design. Rather than leave this portion of DCS design entirely to a follow-on project, an effort was made to use available general information to generate a preliminary

functional design and choose primary system components. Additional work is being done in this area by other researchers.

2. Transmitter Timer

a. General

Under normal operating conditions, the radio will be in the receive mode and only switched to transmit as required. The possibility exists of a catastrophic failure of DCS during a transmission that could lock the radio into a transmit mode, effectively resulting in satellite loss unless the DCS timeout function allowed a transfer of control to the alternate DCS. To preclude this, a programmable interval timer serves as an interface between the microprocessor and the transmitter.

b. Intel 82C54-2 Programmable Interval Timer (PIT)

The 82C54-2 [Ref. 7: pp. 3-83 to 3-99] of Figure 32 was selected based on the following criteria:

1. Radiation tolerant
2. Available in extended temperature range
3. Low power

c. Operation

Capable of handling clock inputs of 10 MHz, the Intel PIT has six programmable modes and three independent 16-bit counters, although current operations required only one counter and one mode (mode 0: interrupt on terminal count).

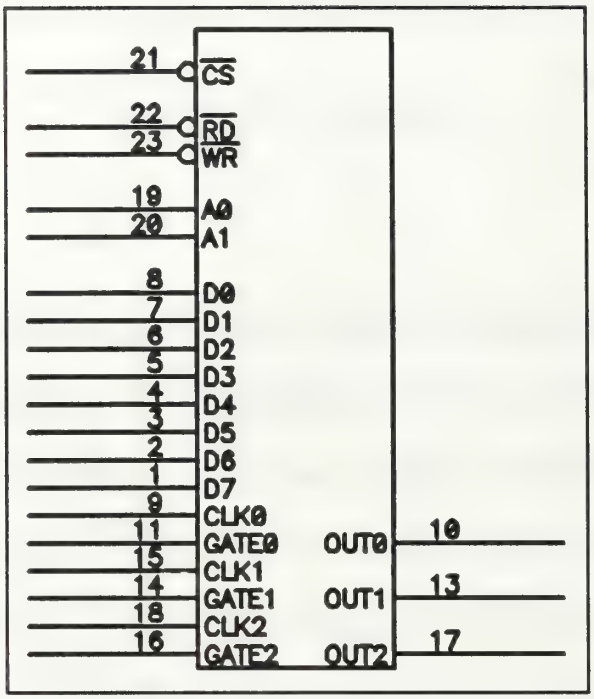

Figure 32 82C54-2

The data pins of the PIT (D0-D7) are connected to the octal transceiver of Section III.B.12, while the clock input of counter 0 (CLK0) is tied to clock output (CLKOUT) of the microprocessor. The chip select pin of the device (CS) is tied to the appropriate peripheral chip select pin (PCS3) of the microprocessor (Table 2.1 germane). Read and write pins of the PIT and microprocessor are connected while the counter output (OUT0) is interfaced with the transmitter.

The two address pins of the PIT (A0, A1) are connected to the two least significant bits of the octal transparent latch used to latch address information or access the control word register (00 for counter 0 select, 11 for control word register select). Assuming mode 0 operation, counter 0 selection, and 16-bit binary counter use, the appropriate control word is 00XY0000, with X and Y options shown in Table 5.1.

TABLE 5.1 CONTROL WORD OPTIONS

X	Y	OPERATION
0	0	COUNTER LATCH COMMAND
0	1	READ/WRITE LEAST SIGNIFICANT BYTE ONLY
1	0	READ/WRITE MOST SIGNIFICANT BYTE ONLY
1	1	READ/WRITE MOST SIGNIFICANT BYTE FIRST, THEN LEAST SIGNIFICANT BYTE

The gate enable pin for counter 0 (GATE 0) can be tied low to continuously enable counting, or connected to one of the spare ports of the PPI of the command bus interface should more flexibility (enable/disable capability) be desired .

3. Communications Processing Functionality

a. General

This functional design incorporates known communications requirements and extrapolates spread spectrum demodulator functionality based on limited technical information. As such, it is a preliminary work and provided as advisory assistance for follow-on work. It is anticipated that unprocessed signal data will be provided to the communications section of DCS from the RF system module via dedicated connectivity external to the command bus. Some preliminary work went in to selection of key components.

b. PARAMAX PA-100 Spread Spectrum Demodulator ASIC

A 223-pin device, the PA-100 [Ref. 16] offers a number of programmable parameters to provide flexibility in tracking and acquisition procedures, modulation types, processing gains, loop bandwidths, etc. It incorporates subsystems supporting automatic gain control (AGC), chip and data rate matched filtering and timing recovery, carrier frequency and phase recovery, PN code acquisition and tracking, and data recovery, and is configured and controlled by the microprocessor via an 8-bit controller interface. Peripheral Chip Select 4 (PCS4, Table 2.1 germane) of the microprocessor controls PA-100 activation. As a one-chip solution to the challenge of spread spectrum demodulation, it was selected by Space Systems at NPS to support PANSAT.

c. Functionality

A generalized functional diagram of the DCS communications system is demonstrated in Figure 33.

For incoming traffic, it is anticipated the microprocessor will receive an interrupt from the serial communications controller (SCC) when traffic arrives and the packets are available in the AX.25 protocol. For outgoing traffic, the microprocessor will send data to the SCC. A fully programmable SCC has been selected and is described below.

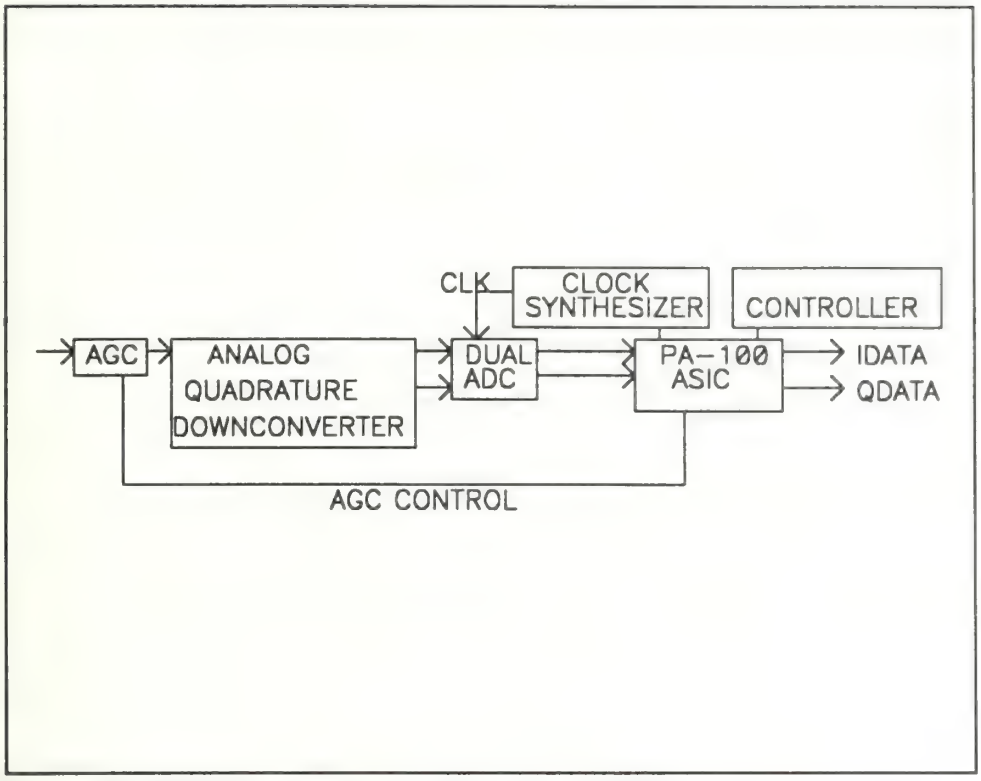

Figure 33 DCS Communications [Ref. 16: p.55]

d. Advanced Micro Devices AM85C30 Serial Communications Controller (SCC)

(1) General selection. The AM85C30 SCC [Ref. 17] is a dual channel, multiprotocol peripheral specifically designed to be used with 16-bit microprocessors. Highly sophisticated and flexible in operation, in keeping with the general nature of this section, salient features only will be addressed. An in depth, detailed description of device operation is provided in the AM85C30 SCC 1992 Technical Manual [Ref. 17]. In addition to the above, other primary selection criteria included:

1. Available in MIL-STD-883 grade
2. DMA (Direct Memory Access) capable

3. Automatic CRC (Cyclic Redundancy Check) generation and detection
4. Internal synchronization
5. Receive and transmit data buffers quadruply and doubly buffered respectively
6. Low power requirements

(2) Operation. The AM85C30 is designed to operate with a microprocessor like the M80C186 and appears to be well suited to interface with the PA-100 as well. A functional diagram of the device is shown in Figure 34.

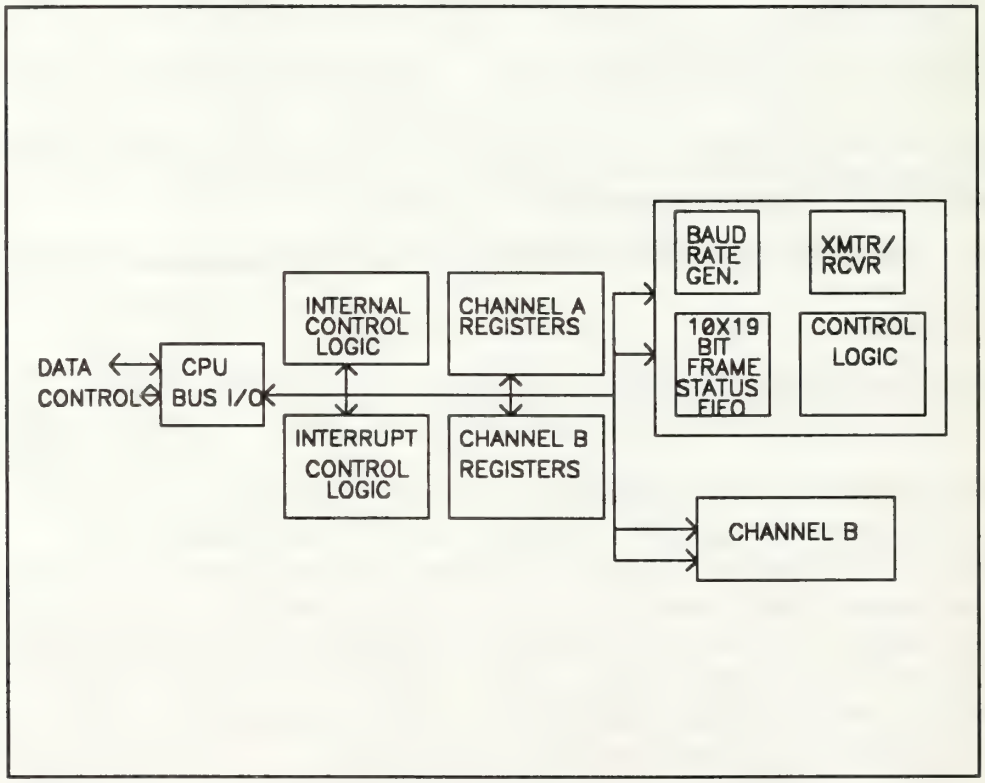

Figure 34 SCC Functional Diagram [Ref. 17: p. 1-5]

Basic connectivity of the device is anticipated to be as follows:

1. The device is enabled by peripheral chip select line 0, PCS0, of the microprocessor (Table 2.1 germane).
2. Channel selection pin A/B is tied high to select A, since only one channel is required.
3. Data lines D0-D7 are tied to the octal transceiver buffering the lower byte of data from the microprocessor.
4. Read and write lines are tied to corresponding lines of the microprocessor.
5. The interrupt request line, INT, is connected via an inverter to one of the interrupt lines of the microprocessor.
6. Interrupt enable pins provided for daisy chaining devices (IE0, IE1) are not required and can be tied off.
7. Serial channel pins will depend on final circuit design and are not addressed.

Further device connectivity and programming is dependent upon determination of communication system operations.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

As a real world design project, PANSAT offers some unique opportunities and perspectives not normally encountered in an academic environment. System design must take into account cost, power constraints, operating conditions in space, autonomous and interactive control of spacecraft systems, and numerous other factors from the mundane, such as contractor delays in delivery of equipment and documentation, to the esoteric, such as determining CMOS vulnerability to radiation. Component selection is a critical part of the overall design process.

Reliability and redundancy have played major roles in the Digital Control System design philosophy. Single point failures are difficult to design around, and power limitations hamper the options available for hardening of components. The current modular concept, wherein major components are duplicated and tied together on a single command bus, offers flexibility in performance and redundancy for the operational lifetime of the satellite.

The design proposed herein for the DCS was made as flexible as possible in regards to standardization of components and in the selection of devices with excess capability wherever possible. A number of the systems the DCS must support are still in the design stage and competing designs and priorities mandated an adaptable hardware system.

B. RECOMMENDATIONS

The design for PANSAT, while making use of proven, off-the-shelf technology, offered some interesting challenges with respect to memory and addressing issues. Follow-on projects will have to deal more closely with communications and processing of on-board telemetry than it was possible to go into at this time.

Follow-on systems should have the opportunity to take better advantage of newer technology than it was possible to do for PANSAT. While project design guidance was for a simple, inexpensive communications relay satellite, it is difficult to get involved with a project like this and not want to go farther. A number of students at the Naval Postgraduate School have turned VLSI designs into operating chips and it may be feasible that a PANSAT follow-on could incorporate devices designed and tested at NPS in satellite subsystems, although this would call for a continuing involvement on the part of planners and designers to avoid redundancy and unwitting obsolescence.

The microprocessor selected is suitable for its planned role on PANSAT. However, considering system tasking, it may be operating at the limit of its capabilities for this project. A more powerful microprocessor would be required in any follow-on satellites with expanded system requirements.

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